T-COM CORPORATION
Digital Telephony Instrumentation

INSTRUCTION MANUAL

DS-1/DS-1C LINE & CHANNEL MONITOR TEST SET

MODEL 320A+

Instrument S/N	:	320A+____
Instruction Manual No.	:	IM320A+01

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* PRELIMINARY ISSUE *
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1. GENERAL INFORMATION

1.1 SCOPE

This instruction and operation manual contains information to install and operate the T-COM Model 320A+ DS-1/DS-1C LINE AND CHANNEL MONITOR TEST SET.

1.2 INTRODUCTION

The model 320A+ is a multipurpose test instrument designed to facilitate the testing and troubleshooting of T-Carrier transmission and digital switching systems interfacing with DS-1 and DS-1C formatted bit streams.

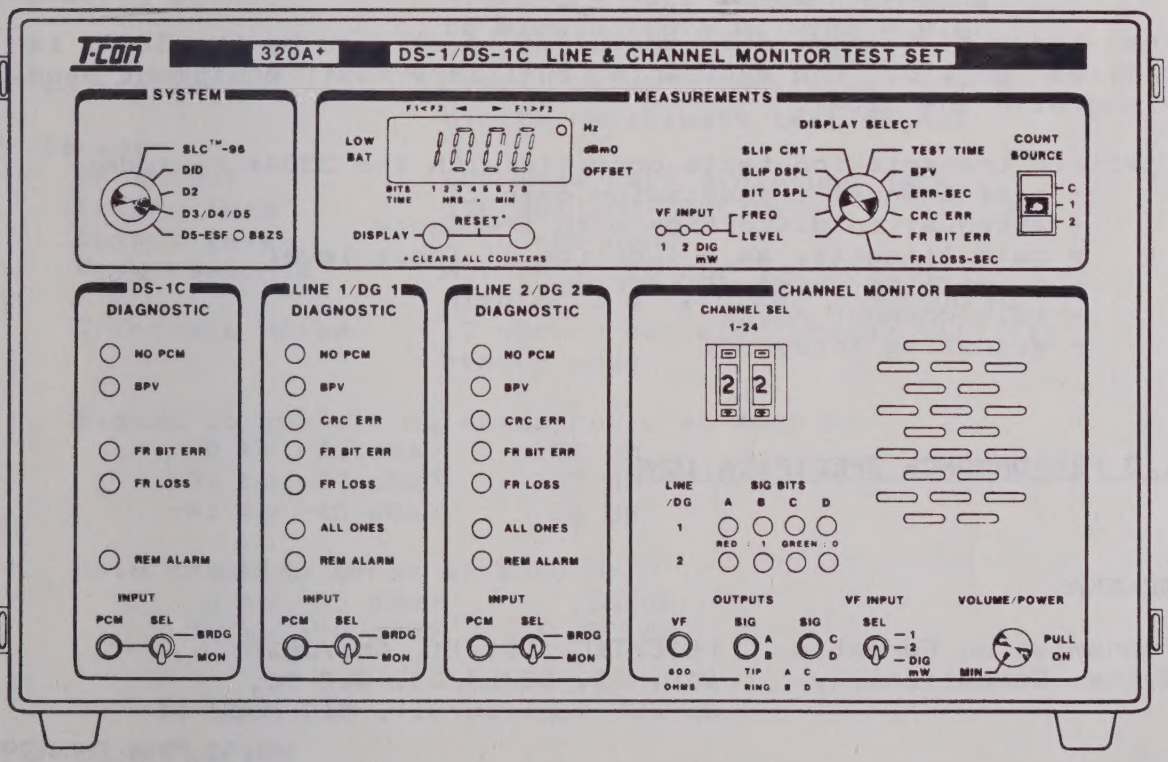

Figure 1.1 Front Panel

The set capabilities are grouped in three sections operating in combination. These sections are:

- the Line Diagnostic (1 DS-1C and 2 DS-1)
- the Channel Monitor
- the Measurement Section

Each Line Diagnostic section provides comprehensive testing of the corresponding PCM bit stream for transmission impairments as well as identification of specific alarm messages.

The Channel Monitor section permits the characterization of voice transmission of the A/D (analog to digital) transmit half channel as well as the monitoring of signaling states associated with a VF channel for each bit stream under observation.

The Measurement section provides for the individual capture of impairment events associated with each PCM line and the display of the events upon request. In addition, the built-in TMS capability makes it possible to measure both the level and the frequency of the signal found in a selected VF channel.

The range of transmission measurements allowed by the 320A+ is limited only by the available auxiliary test equipment used along with the 320A+.

Specific transmission tests possible with the 320A+ include:

- half channel transmission gain
- attenuation distortion with frequency
- gain linearity as a function of input level
- quantizing noise distortion
- idle channel noise
- signaling integrity

1.3 PERFORMANCE SPECIFICATIONS

GENERAL

Transmission Format	DS1C/T1C, DS1/T1, AMI/B8ZS
System Compatibility	D1D, D2, D3/D4/D5, SLC-96, D5-ESF (option 01), MiC Mode II

PCM DIAGNOSTICS SECTIONS

Input connectors	Miniature jack
Input modes	Bridging (1000 ohms) Monitoring (100 ohms)

Input level	2.0 to 4.0 V base to peak
Test display	50 ms nominal per event
Test Indicators	
NO PCM	≥ 20 consecutive 0's for T1
	≥ 100 consecutive 0's for T1C
BPV	consecutive 1's of same polarity
CRC ERR	CRC-6 error (option 01)
FR BIT ERR	Error in frame bit time slot
FR LOSS	Out of frame lock
ALL ONES	All bits are 1 for 50 ms min
REM ALARM	B2 = 0 for 50 ms min or ESF alarm code (option 01) X bit is 0 for T1C

CHANNEL MONITOR SECTION

Channel selection	Anyone of 24 w/ code switch
Signaling display	State of A, B, C, & D bits for both DS1 lines simultaneously
Signaling output	Miniature jack contact closure to sleeve Tip = A, Ring = B & (option 01) Tip = C, Ring = D
VF source select	Line 1, line 2, built-in digital milliwatt test signal
VF Decoder	
VF output	600 ohms bal/ miniature jack
Return loss	>28 dB/ 300-3300 Hz
Output level	3 to -55 dBm0
Freq response	Within ± .20 dB/ 300-3000 Hz
	Within .3 & -1.0 dB/ 200-3300 Hz
Intrinsic noise	13 dBrnc0 max with steady 11111111 binary code

Signal to quantizing noise ratio at 1010 Hz

0 to -30 dBm0	>33 dB
-31 to -40 dBm0	>27 dB
-41 to -45 dBm0	>23 dB

Gain tracking error at 1010 Hz

0 to -35 dBm0	± .30 dB
-36 to -50 dBm0	± .50 dB

SPEAKER AMPLIFIER

Gain	Continually adjustable to 40 dB
Freq response	Within 2.0 dB/ 300-3000 Hz
Power	Up to 150 mW

MEASUREMENT SECTION

Display type	Seven segment LED
Display mode	
LEVEL	VF signal level
FREQ	VF signal frequency
BIT DSPL	Instantaneous 8-bit state display
SLIP DSPL	Frame slippage display
SLIP CNT	Frame slip count
TEST TIME	Elapsed time since reset
BPV	Bipolar violation count
ERR-SEC	Errored second count
CRC ERR	CRC-6 error count
FR BIT ERR	Frame bit error count
FR LOSS-SEC	Frame loss count
Counting range	0000 to 9999 for all counters

TMS

Frequency range	100 to 3990 Hz
Freq accuracy	± 1 Hz w/ level >-40 dBm0
Level range	3.2 to -59.9 dBm0
Level accuracy	± .15 dB/ 3 to -40 dBm0
	± .30 dB/-41 to -50 dBm0
	± .50 dB/-51 to -59.9 dBm0
Offset	Long term DC average >10 counts in scale of 8031
Measurement rate	2 per second

AUXILIARY ACCESS

DS1 Timing signals	As required to access: - SLC-96 data link messages - ESF data link messages and interface with T-COM model 515A

DSO DATA ACCESS INTERFACE (option 03)

Data	64 kb/s selected channel content
Timing	64 kHz and 8kHz clocks

POWERING

AC power	108-126 VAC, 50-60 Hz/ 12W
Battery back-up (option 04)	12 V, 1.2 Ah NiCad rechargeable 3 hrs nominal of continuous use with display off Recharge time: 14 hours nominal

MISCELLANEOUS

Operating temp	10 to 40°C (50 to 104°F)
Storage temp	-30 to +70°C (-22 to 158°F)
Humidity	Up to 90% non-condensing
Dimensions	8.12"(H) x 13.5"(W) x 11.5"(D) (D = 13" w/ Front cover)
Weight	15 lbs (6.8 kg) with battery

ORDERING INFORMATION

Model 320A+ includes	Basic instrument with front cover, 6 foot AC power cord and one operation manual
Option 320A+-01	Provides extended framing (D5-ESF) compatibility
Option 320A+-03	Provides DS0 data access interface for KS 20908 data test set
Option 320A+-04	Provides battery back-up
Option 320A+-R	Rotary power switch/volume control (instead of push-pull). Change not indicated on front panel.

*** Options can be combined as needed ***

Accessories:

1886-001	Canvas Carrying Case
1886-002	Polyethylene Shipping Case
1690-001	4 Foot Patch Cord Terminated with Miniature plugs
1690-002	4 Foot Patch Cord Terminated with Miniature and 310 plugs
1694-001	Miniature to 310 Adapter Plug
IM 320A+-01	Extra Instruction Manual
2700-021	4-foot, 9-conductor signaling cable assembly
2750-032-P	Rack Mount Kit 19"
2750-033-P	Rack Mount Kit 23"

Replacement Parts:

1700-012	Power Cord
1500-004	Fuse 1/4A FB
1500-005	Fuse 1-1/2A FB
2751-022	Front Cover Assembly
2360-001	Battery Set

2. INSTALLATION

2.1 INTRODUCTION

This section contains information and instructions for installing the model 320A+. Included are initial inspection procedures, power requirements, instructions for rack mounting installation and repacking for shipment.

2.2 INITIAL INSPECTION

Inspect the shipping container for damages. Should any damage be found, the container must be kept until all contents of the shipment have been checked for completeness and the instrument has been checked mechanically and electrically. Procedures for checking electrical performance are given in Section 6. If the contents are incomplete, if there is mechanical damage or defect, or if the instrument does not pass the performance tests, notify your T-COM Representative.

If the shipping container is damaged, notify the carrier as well as the Representative. Keep the shipping material for the carrier's inspection.

2.3 PREPARATION FOR USE

Powering -- The model 320A+ operates from the 120 VAC line. When the 320A+ is equipped with option 04 the built-in battery provides for powering of the set for several hours.

Notes on AC operation:

1. A six-foot, three conductor AC cord is supplied with the model 320A+.

2. AC power connection to the 320A+ is made via the three prong AC inlet located on the 320A+ rear panel.

CAUTION

Removal of the ground pin from the supplied AC power cord constitutes a safety hazard and voids the warranty.

Notes on battery operation:

1. The rechargeable battery provided as part of option 04 is normally shipped from the factory in a partially charged condition. Before a full charge can be obtained it is recommended to place the battery under charge for a period of 14 hours.

2. The battery is recharged automatically when the set is connected to the AC line; whether the set power switch is ON or OFF does not affect the battery charging rate.

3. In the event of AC power failure, if the power switch is ON, the set will be powered from the battery without interruption.

4. When a fully charged battery no longer sustains operation of the set for at least two hours, a new battery set should be installed. A new battery set provides a minimum of three and one half hours of continuous operation.

5. When replacing the battery, both battery sticks must be replaced at the same time to ensure satisfactory operation.

Battery replacement

The set of batteries is easily replaced in the field using a #1 philips screwdriver (compatible with No. 4 and No. 6 screws). Refer to Figure 2.1 and follow the steps listed on page 2-2. When replacing the battery pack use exclusively the T-COM battery set, part number: 2360-001

CAUTION

The use of any other make or part number, or modification to the batteries may result in damage to the instrument and void the warranty.

Step 1 Disconnect any patch cord from the set front panel jacks and make sure the AC power cord is disconnected from the set.

Step 2 Unscrew and remove the six No. 4 philips screws holding the rear panel to the rear bezel. These screws are located along side the edges of the rear panel.

Step 3 Pull gently on the rear panel legs to remove the rear panel from the unit. The cable connecting the rear panel mounted power supply assembly to the mother board must be disconnected before the rear panel can be freed

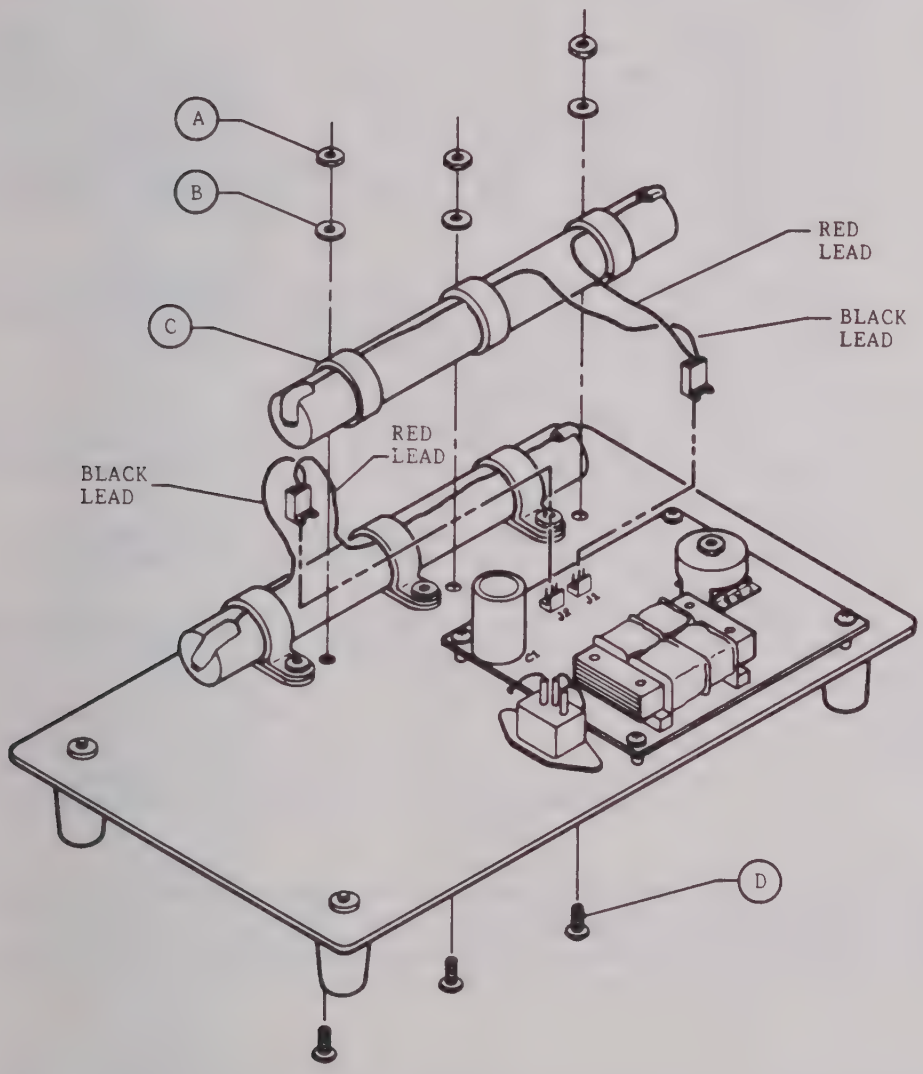

Figure 2.1 Internal view showing battery replacement

from the instrument. To disconnect the cable, move the rear panel in such a way that a hand can access the cable-connector near the bottom left of the unit. Hold the connector and firmly pull upward vertically from the mother board to free the connector from the male header.

Step 4 Disconnect the two battery sticks from the power supply assembly by unplugging J1 and J2.

Step 5 Unscrew and remove the six No. 6 philips screws securing the battery clamps to the rear panel and discard the batteries.

Step 6 Remove the new battery packs from the shipping protection and for each battery install the 3 clamps over the conductors and the battery. Be sure that the conductors are aligned in the grooves in the 3 felt strips and place the clamps over these strips. Also be sure that the red and black leads are placed as shown in Figure 2.1.

Step 7 Reconnect each battery connector respectively to J1 and J2 on the power supply assembly. Either battery can be connected to either J1 or J2.

Step 8 The power supply cable must be properly installed for the set to operate; make certain before attempting to plug it into the header that perfect pin alignment is obtained.

Step 9 Carefully replace the rear panel and secure it with the six No. 4 philips screws.

The new battery is normally discharged and should be fully charged before using the instrument.

CAUTION

Do not dispose of the battery in an open flame as possible explosion may result in personal injury.

Rack mounting -- When the instrument is to be installed in a relay rack, the appropriate set of rack mounting brackets must be installed on the sides of the instrument.

The mounting brackets part numbers are:
for 19" wide rack: 2750-032-P
for 23" wide rack: 2750-033-P

Mounting bracket installation -- Each bracket is secured on the opposite sides of the instrument by a set of two philips pan head 10-32 screws as shown on Figure 2.2 below.

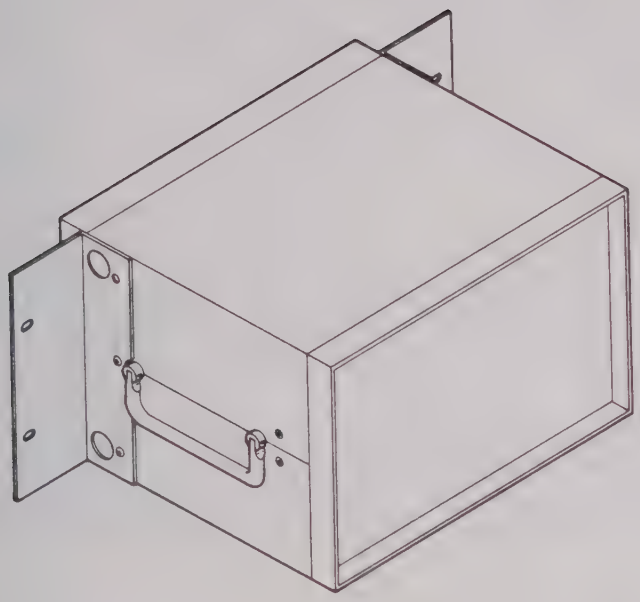

Figure 2.2 Mounting bracket installation

2.4 DSO ACCESS INTERFACE RETROFITTING INSTRUCTIONS

The DSO access interface, option 03, can be installed in the field by any mechanically minded person following the steps of the retrofitting procedure below. It requires approximately 10 minutes and a philips screwdriver suitable for number 4 screws to carry out the entire procedure.

Important note: The DSO interface assembly capacitive adjustment (CT1) is critical and one must be careful not to alter its setting. If the setting has been changed refer to section 7 of the manual for calibration instructions.

CAUTION

When carrying out the retrofitting procedure outlined below, the set must be disconnected from the AC line and the set power switch must be turned OFF. Failure to comply with this requirement can result in harm to the operator and/or the test set.

Step 1
Remove the six screws securing the rear panel to the bezel. These screws are located on the periphery of the rear panel. Gently pry the panel loose from the bezel and let it rest horizontally on the four legs. Unplug the flat ribbon cable connecting the power supply board to the mother board by holding on firmly to the 20 position connector and by pulling vertically away from the mother board.

Step 2
Remove the six screws securing the dummy panel to the test set rear panel and place the dummy panel aside. The dummy panel covers the large cavity on the right side of the rear panel, and is of no further use once the DSO option is installed.

Step 3
Unwrap the DSO interface assembly and place it on the inside surface of the rear panel over the cavity previously covered by the dummy panel. Secure the DSO interface assembly to the rear panel with six screws. Do not overtighten.

Step 4
Place the rear panel horizontally on its legs and orient it in such a way that the power supply ribbon cable and the DSO interface assembly ribbon cable are aligned respectively with their mating header on the mother board. Connect the two ribbon connectors to the corresponding male headers, making certain that they are properly aligned and fully engaged.
Note: alignment offset in either connector can result in substantial damage to the instrument.

Step 5
Gently fold back the rear panel into its normal resting position against the bezel and secure it in place with the six remaining screws.

This completes the DSO assembly retrofitting procedure. Prior to placing the test set back into service, it is recommended to carry out the self testing procedure described in section 3.6 of the instruction manual to ensure operational integrity.

2.5 REPACKING FOR SHIPMENT

The use of the original shipping carton and packing material is highly recommended. If the original packing material is not available, you may use any strong container. Wrap the instrument in heavy paper or a plastic bag and surround it with three or four inches of shock absorbing material to cushion it firmly and prevent movement inside the container.

Note: Your authorized T-COM representative is ready to assist you in any situation and you are always welcome to get directly in touch with the T-COM service department:

Customer Service
T-COM
805 East Middlefield Road
Mountain View, CA 94043
(415) 964-3415

All equipment returned to the factory must be accompanied by a manufacturer's Return Authorization number. In order to get an RA number, customers should call in or write, with the model and serial numbers of equipment to be returned, **PRIOR** to shipment. A number will be issued, which will be referenced in both the packing slip and the purchase order associated with the equipment. Include with the instrument a comprehensive description of the problem(s) encountered to ensure that the instrument is satisfactorily repaired.

3. OPERATION

3.1 INTRODUCTION

This section provides operating information, explains the functions of the 320A+ controls, connectors and indicators and describes measurement capabilities of the instrument.

3.2 FRONT PANEL FEATURES

The 320A+ front panel features are described below. The description numbers match the numbers in Figure 3.1.

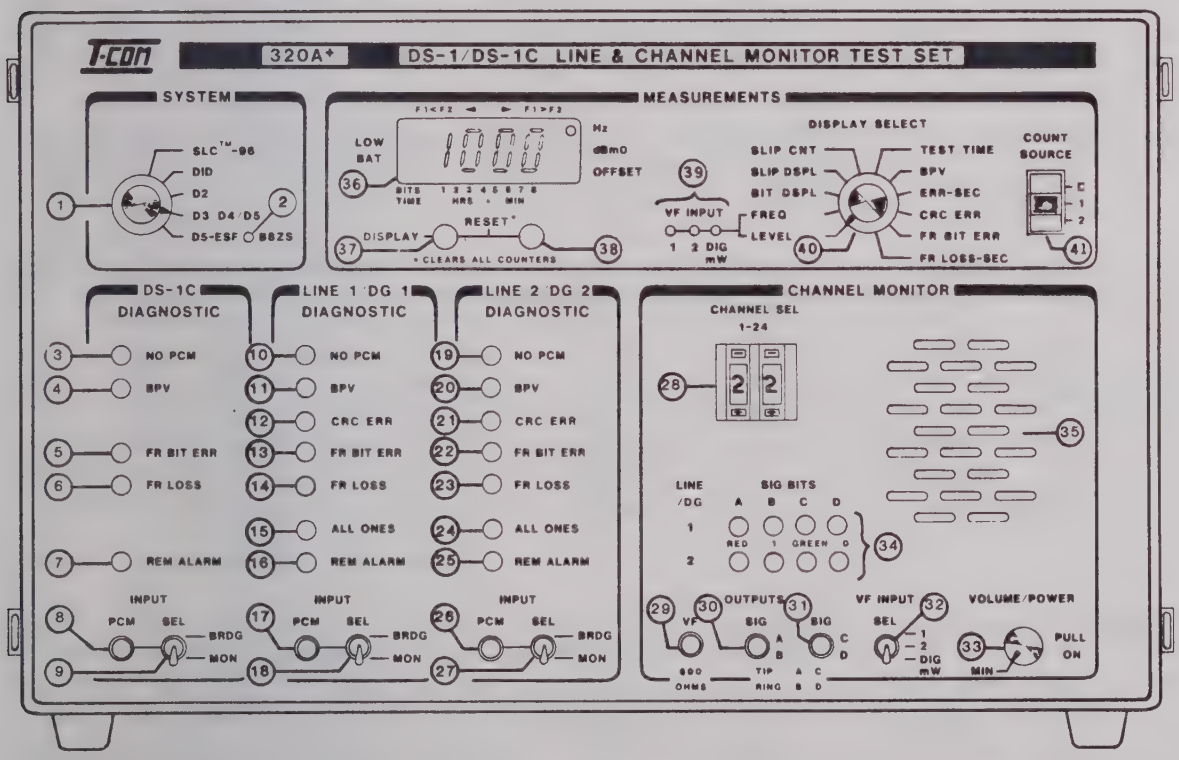

Figure 3.1 Front Panel Features

System section

1 **SYSTEM SELECTION** -- This switch provides for compatibility selection with several D-bank channel numbering sequences and framing formats.

2 **B8ZS** -- This LED is lit when the B8ZS code is detected on either DS1 PCM input bit stream, independent of the system selection setting.

DS1C Diagnostic Section

3 **NO PCM** -- This LED flashes for 50 ms when a string having over 100 consecutive 'zero' bits is detected. It is lit continuously when the PCM bit stream is not compatible with the input configuration requirements.

4 **BPV** -- This LED flashes for 50 ms when two consecutive 'one' bits having the same polarity are detected.

5 **FR BIT ERR** -- This LED flashes for 50 ms when the state of a framing bit (alternating 1 and 0 pattern) is in error. This LED is operational only when FR LOSS LED is not lit.

6 **FR LOSS** -- This LED is lit when framing is not acquired or has been lost. Framing loss occurs when two out of five frame bits are in error.

7 **REM ALARM** -- This LED is lit when the remote alarm code is detected (X bit state is zero).

8 **PCM INPUT** -- This miniature jack receives the PCM bit stream to be monitored by the diagnostic section.

9 **INPUT SEL** -- This switch configures the PCM input to interface with the PCM line either in a bridging mode (BRDG) or via a high impedance monitor jack access (MON).

Line 1 Diagnostic Section

10 **NO PCM** -- This LED flashes for 50 ms when a string having more than 17 +/- 2 consecutive 'zero' bits is detected. It is lit continuously when the PCM bit stream amplitude is not compatible with the input configuration requirements or when the PCM line is oscillating.

11 **BPV** -- This LED flashes for 50 ms when two consecutive 'one' bits having the same polarity are detected. If the line carries B8ZS, only the illegitimate bipolar violations are displayed.

12 **CRC ERR** -- This LED flashes for 50 ms when a CRC-6 discrepancy is detected, indicating that one or more bits were in error during the transmission of the previous 24 frames. This LED is operational only when the EFS mode is selected.

13 **FR BIT ERR** -- This LED flashes for 50 ms when the state of a framing bit (F_T) is in error. This LED is operational only when FR LOSS LED is not lit.

14 **FR LOSS** -- This LED is lit when framing is not acquired or has been lost. Framing loss occurs when two out of five frame bits are in error.

15 **ALL ONES** -- This LED is lit when the monitored PCM bit stream consists of an uninterrupted sequence of 'one' bits during at least 50 ms.

16 **REM ALARM** -- This LED is lit when the remote alarm code is detected. For SLC-96, D1D, D2, D3/D4/D5 this alarm code requires that bit two in each channel is set to zero state for at least 50 ms. For D5-EFS this alarm code requires that the data link message consist of a minimum of 14 consecutive sequences of 8 'ones' followed by 8 'zero' bits.

17 **PCM INPUT** -- This miniature jack receives the PCM bit stream to be monitored by the diagnostic section.

18 **INPUT SEL** -- This switch configures the PCM input to interface the PCM line either in a bridging mode (BRDG) or via a high impedance monitor jack access (MON).

Line 2 Diagnostic Section

Items 19 through 27 are identical to items 10 through 18, respectively, in the Line 1 Diagnostic Section.

Channel Monitor Section

28 **CHANNEL SEL** -- This set of code switches selects any one of the 24 channels in the DS1 bit stream. When a non-existent channel number is selected (i.e. 34) the channel monitor section is not functional.

29 **VF OUTPUT** -- This miniature jack accesses the decoded VF content of the selected channel. The level on this output is normalized such that 0dBm = 0dBm0, when a 600 ohm load-termination is provided.

30 **SIG A/B OUTPUT** -- This miniature jack accesses the A and B signaling states associated with the channel selected from line 1 or line 2 with switch 24. A state 'one' for SIG A yields a contact closure between tip and sleeve. A state 'one' for SIG B yields a contact closure between ring and sleeve. When switch 24 is set on DIG mW or when framing is lost on the selected line this jack is not functional.

31 **SIG C/D OUTPUT** -- This miniature jack accesses the C and D signaling states associated with the channel selected from line 1 or line 2 with switch 24. A state 'one' for SIG C yields a contact closure between tip and sleeve. A state 'one' for SIG D yields a contact closure between ring and sleeve. When switch 24 is set on DIG mW or when framing is lost on the selected line, or when EFS is not selected this jack is not functional.

32 **VF INPUT SEL** -- This three position switch selects the VF source that may be listened to and measured by the TMS in the measurement section. By selecting DIG mW, a built-in source can be heard on the speaker and used for verification of the instrument operation and calibration.

33 **VOLUME/POWER** -- This knob controls the loudspeaker amplifier gain as well as the instrument's powering. To power the instrument, the knob must either be pulled out or twisted clockwise, depending on the option for this switch.

34 **ABCD SIG BITS** -- These 8 bicolor LED's display the signaling states associated with the selected channel for each line, independent of the setting of switch 32. Signaling bits C and D are lit only when EFS mode is selected.

35 **SPEAKER**

Measurements Section

36 **DISPLAY** -- 4 seven-segment digits and 2 discrete LED's provide for the measurement display along with the indication of units. Two additional LED's are used to display respectively the presence of offset and the low state of charge of the battery (option 04 only). The OFFSET LED is lit when the longterm average of the PCM samples associated with the monitored channel exceeds 10

samples associated with the monitored channel exceeds 10 counts, indicating a misadjustment or defect of the channel encoder circuit. The LOW BATTERY LED is lit when the set is operating under battery power and the end of charge is near.

37 **DISPLAY** -- This switch has a dual purpose. (1) When operating under battery power the display is normally off to save energy. By depressing this switch briefly the display is turned on for 15 seconds nominal. (2) When operating under battery power or from the AC line this switch is used jointly with the switch 38 to clear all event counters and reset the slippage detector.

38 **RESET** -- This switch must be depressed simultaneously with switch 37 to clear all event counters and reset the slippage detector.

39 **VF INPUT** -- These three miniature LED's provide indication/reporting of the VF source selected by switch 32 in the Channel Monitor section.

40 **DISPLAY SELECT** -- This switch selects the type of measurement displayed as follows:

LEVEL	:	signal level (dBm0) in selected channel
FREQ	:	signal frequency (Hz) in selected channel
BIT DSPL	:	instantaneous 8-bit state associated with selected channel
SLIP DSPL	:	accumulated frame slip count
TEST TIME	:	elapsed time (HH:MM) since last reset
ERR-SEC	:	total number of seconds in which one or more BPV or loss of PCM or CRC error (if in ESF mode) occurred
CRC ERR	:	accumulated number of CRC-6 errors (ESF mode only)
FR BIT ERR	:	accumulated number of frame bit errors
FR LOSS-SEC	:	accumulated number of seconds during which framing was lost

Remark: When a selection is not meaningful the display reads '-OO-'.

41 **COUNT SOURCE** -- This switch selects the line, '1' for LINE 1, '2' for LINE 2, 'C' for DS1C Line, for which impairment events are displayed; in effect switches 40 and 41 combine to display specific events associated with a given line.

3.3 REAR PANEL FEATURES

The 320A+ rear panel features are described below. The description numbers match the numbers on Figure 3.2

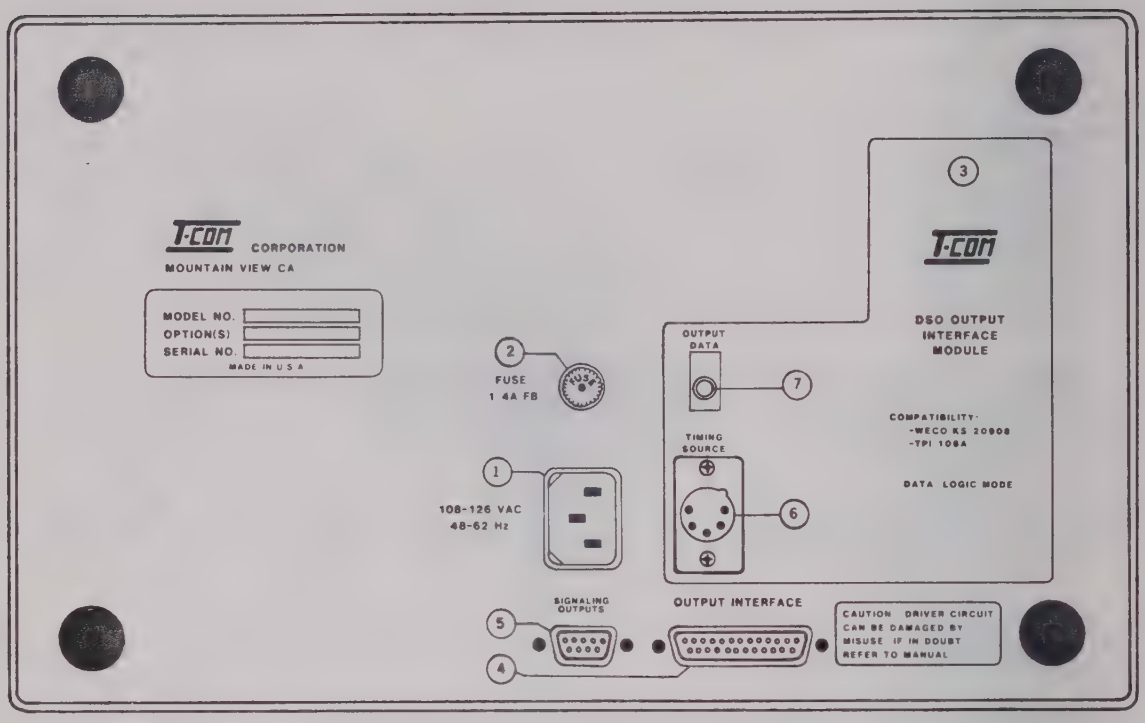

Figure 3.2 Rear Panel Features

1 **115 VAC** -- This three-prong inlet is used to connect the supplied AC power cord to a commercial AC source.

2 **Fuse** -- 1/4 A Fast Blow

3 **Optional DSO interface panel** -- When option 03 is not isntalled, this panel is blank.

4 **25 position female connector** -- This connector provides access to the timing signals required to obtain the data link messages in SLC-96 and ESF formatted transmissions.

5 **9 position female connector** -- This connector provides access to the signaling states associated with the selected channel in both DS1 lines.

6 **5 pin connector** -- This connector provides access to the timing signals required by the KS 20908 to properly decode the 64 kb/s data stream available at jack 7.

7 **DSO Data output jack** -- This jack delivers the recovered 64 kb/s data in the selected channel.

3.4 OPERATIONAL CAPABILITIES

The Model 320A+ offers the following general capabilities

- Independent and dedicated impairment diagnostics for one DS1C and two DS1 lines.
- Capture and retrieval of diagnostic data.
- PCM channel access with VF and signaling decoding.
- Level and frequency measurement of the selected channel signal content.

These capabilities can be used alone or in combination, in a variety of situations to monitor and analyze the PCM transmission through a system, as well as to perform half channel transmission evaluation.

3.4.1 T-Carrier PCM transmission diagnostic

To monitor a DS1C Line for transmission impairments the PCM input jack 8 in figure 3.1 must be connected across the line. The INPUT SEL switch must be set to BRDG when the input is patched directly across the PCM line; it must be set to MON when the input is patched to a monitor jack. (A monitor jack has its tip and ring connected to the PCM line via a 430 ohm resistor.) To ensure satisfactory results, it is recommended that patch length not exceed 10 feet.

To monitor a DS1 Line for transmission impairments, either PCM input jack 17 or 26 in figure 3.1 must be patched to the PCM line. The appropriate input selection switch 18 or 27 in figure 3.1 must be set to ensure compatibility with the bridging mode or with connection of the set via a high impedance monitor jack. The INPUT SEL switch must be set to BRDG when the input is patched directly across the PCM line; it must be set to MON when the input is patched to a monitor jack. For DS1 rate, patch cord length is not critical in either configuration as up to 800 pF of cabling capacitance can be tolerated by the set.

If a DS1C Line is monitored and plugs are not inserted in jacks 17 and 26, LINE 1/DG1 and LINE 2/DG2 Diagnostic sections provide the diagnostic respectively for each D-group demultiplexed from the DS1C bit stream. Alternatively it is

possible to monitor, at the same time, a DS1C and a DS1 bit stream. When a DS1 bit stream is monitored, the corresponding diagnostic section characterizes the externally applied DS1 signal instead of the demultiplexed D-group. This feature provides for comparing the DS1 bit streams prior to and after multiplexing by an M1C multiplexer as is illustrated in figure 3.3.

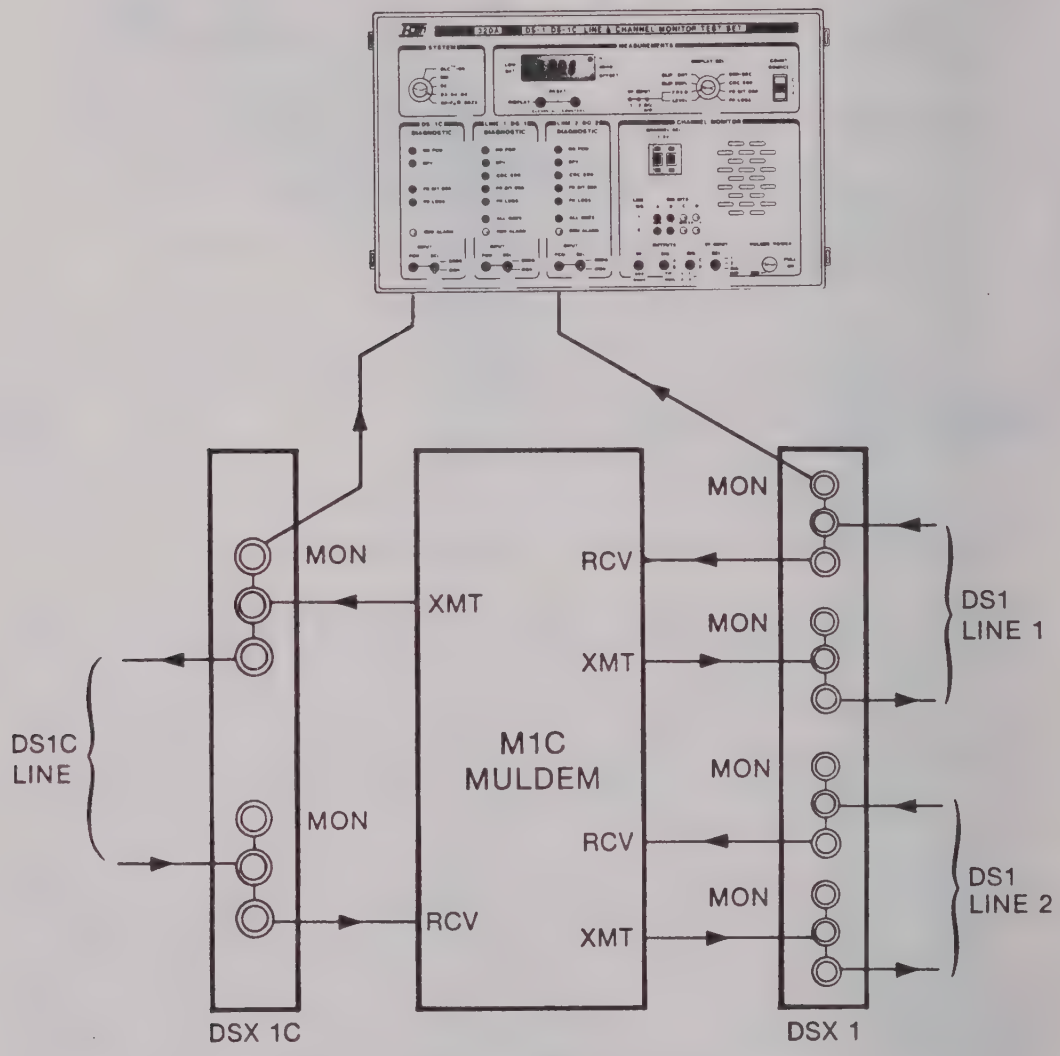

Figure 3.3 Muldem Encoding/Decoding Integrity Testing

3.4.2 DS1 Slippage Detection

Slippage occurring between two non-synchronous DS1 bit streams can be observed in real time on the measurement section display by setting the DISPLAY SEL switch 40 to SLIP DSPL.

Figure 3.4 a-i shows the two upper vertical segments for each of the four digits used to display the slippage.

The displayed slippage is that occurring between the two bit streams monitored by LINE 1/DG1 and LINE 2/DG2 diagnostic sections without regard for their origin.

Figure 3.4a Quiescent Position

Fig. 3.4a shows the legitimate display obtained under either of the following conditions:

1 - reset has just been entered
2 - a full slip (125us) has been completed
3 - the two PCM bit streams are synchronous

If the two bit streams are synchronous and jitter on the transmission is moderate, the quiescent position shown in Fig. 3.4a must prevail for any length of time. Should either bit stream be momentarily lost the display is turned off to avoid yielding erroneous information. If the two bit streams are not synchronous two conditions can exist: either F1 < F2 or F1 > F2 (F1 and F2 are the clock frequencies associated with Line 1 or DG1 and Line 2 or DG2, respectively).

Figures 3.4b through 3.4e show successive snapshots of the display obtained when F1 is less than F2.

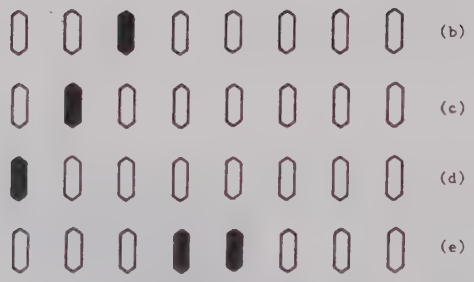

Figure 3.4b-e Frame Slippage when F1 < F2

A frame slip (125us) count is obtained when the display passes from 3.4d to 3.4e

Figure 3.4f through 3.4i show successive snapshots of the display obtained when F1 is greater than F2.

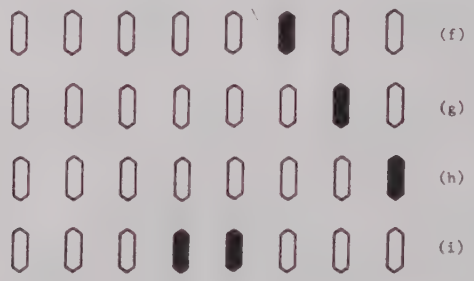

Fig. 3.4 f-i Frame Slippage when F1 > F2

A frame slip (125us) count is obtained when the display passes from 3.4h to 3.4i.

The segments position with respect to slip length is approximately linear. The actual proportions are as follows: referring to fig. 3.4a

0 to 1 : 16% of 125us or 20 time slots
1 to 2 : 28% of 125us or 35 time slots
2 to 3 : 28% of 125us or 35 time slots
3 to 0 : 28% of 125us or 35 time slots

3.4.3 Capture and Retrieval of Diagnostic Data

Several events associated with the DS1C Line, Line 1 and Line 2 are captured and accumulated in distinct counters for retrieval when needed; independent of the measurement section display selection switch setting. Each of these counters is capable of storing up to 10,000 events. Six types of events are stored:

- Bipolar violations
- Errored seconds
- CRC errors (ESF mode only)
- Framing bit errors
- Frame loss-seconds
- Frame slip counts

Bipolar violations are counted for each line separately. (A bipolar violation occurs when two consecutive 'one' bits have the dame polarity.)

For DS1C, the errored-second counter is incremented by one count when during a given second one or more BPV's occur and /or PCM carrier loss occurs. For DS1, the errored-second counters are incremented differently depending upon the system selection. When the system selection is SLC-96, D1D, D2, or D3/D4/D5 the errored-second counter is incremented by one count when during one second one or more BPV's occur and or PCM carrier loss occurs. If the system selection if D5-ESF, the errored-second counter is incremented by one count when during one second one or more BPV's occur and/or PCM carrier loss occurs and/or one or more CRC-6 errors occur.

The CRC error count is provided only when the system operates in the D5-ESF framing format and reflects the number of CRC-6 error flags. A CRC-6 error flag indicates that during the transmission of the previous 24 frames, one or more bits was in error.

For DS1C, the frame bit error counter is incremented by one count for each 'F' bit error. For DS1, the frame bit error counters are incremented differently depending upon the system selection. When the system selection is either SLC-96, D1D, D2, D3/D4/D5, the frame bit error count accumulates errors in the F_T bit. When the system selection is D5-ESF, all errors associated with the framing bits are accumulated.

The frame loss-second count is incremented by one count for each second in which a frame loss condition occurs, whether the frame loss duration lasts a full second or only a fraction of a second. A frame loss condition results when the instantaneous density of frame bit errors reaches 2 in 5.

During a frame loss condition, both the CRC ERR and the FR BIT ERR counters are prevented from incrementing.

The slip counter is incremented when a full 125us slip between the two monitored bit streams from a reference position has taken place. The slip counter is disabled whenever either bit stream is lost. The slip counter cannot be incremented at a rate exceeding one slip per 10 seconds.

Retrieval for display of an individual event count is obtained by setting the measurement section display selection and count source switches as required.

While the slip count displayed is independent of the count source selection switch setting, the counts associated with BPV, ERR-SEC, CRC ERR, FR BIT ERR, and FR LOSS-SEC are distinct for each line.

Any counter may be incremented while its content is being displayed. Should any counter have received a total count exceeding 9999 events the display indicates overflow for the counter by flashing '9999'. When the display selection switch is set either on an unassigned position or to a setting that is not consistent with the system selection (i.e. CRC ERR with system selection D2, or with the DS1C line) the symbol '-OO-' is displayed. This symbol stands for 'not assigned'. All counters are reset and the slippage detector initialized by simultaneously pressing the two reset switches.

3.4.4 Digital channel access and decoding

To access, decode and monitor the content of a channel in a monitored DS1 PCM bit stream refer to Figure 3.1 and set the switches as follows:

Set switch 1 according to the D-Bank type generating the bit stream.

Set switch 18 and/or 27 either to BRDG or MON as appropriate. The BRDG setting must be used when the access is patched directly across the line. The MON setting must be used when the access is made via a monitor jack. A monitor jack tip and ring are typically connected to the line via a set of 2 resistors of 430 ohms.

Set switch 28 to the desired channel number.

Set switch 32 to select the DS1 line from which the channel is selected: 1 for line 1, 2 for line 2.

For the selected channel, the channel monitor section provides:

- the states of each signaling bit for each monitored line
- the calibrated VF level corresponding to the decoded VF bits from the selected line
- a loudspeaker output for the decoded VF
- the electrical output for the signaling states associated with the selected line.

Outputs from this section may be applied in various ways. The encoder signaling accuracy can be tested by observing the states of the signaling bit response to known input signaling states. The corresponding electrical signaling output permits dial pulse distortion measurement using commonplace signaling test sets.

By using the calibrated VF output level it is possible to evaluate gain linearity, frequency response, idle encoder noise and distortion. Similarly, the loudspeaker output may be used to identify and make subjective evaluation of the content of a selected channel.

Remarks: To perform the measurements indicated above, access to the originating channel bank is required, along with the use of a test oscillator and a noise-and-level measuring set. Set-ups required to perform these measurements are given in section 3.5.

3.4.5 Level and Frequency Measurement of the Selected Channel Signal Content

The built-in TMS capability provides for the measurement of level and frequency of the signal in the selected VF channel in either line 1 or line 2. Excessive DC offset level in that channel can also be detected. The selection of line 1 or line 2 is made by setting switch 32 accordingly; this selection is also reported in the measurement section by LED's 39.

By setting the display selection switch (40) to either LEVEL or FREQ respectively, the level in dBm0 or the frequency in Hz is displayed.

Remarks:

If the level is <-40 dBm0 the frequency of the signal cannot be guaranteed and the following message is displayed instead: 'LO L'

If the level is <-60 dBm0 its accuracy cannot be guaranteed and the following message is displayed instead: 'LO-L'

If the level exceeds 3.2 dBm0 it will be distorted and the following message is displayed: 'OL'

Should a problem develop while using the TMS capability a self diagnostic message is provided in lieu of the measurement. The diagnostic message shall be 'E2 x' with 'x' a specific character.

The level or frequency measurement of the signal contained in a selected channel is meaningful only when framing prevails. Should framing be lost on the line for which the channel content is measured, the display will go blank and remain blank until framing is regained.

Offset:

When the display selection is LEVEL, the LED labeled OFFSET provides an indication of excessive DC offset introduced typically by the VF encoder in the transmit signal source (typically a channel unit). The actual origin of the offset may be either improper adjustment of the encoder offset compensation or a systematic encoding error (i.e. stuck bit). In any event, this offset can cause transmission gain mistracking and signal distortion. When the offset light is turned on, the level displayed is greater than the actual AC level sent by the encoder. If the offset is very large, the frequency measurement can be impaired. The offset LED is lit only when the two following conditions are met:

1. The long term average value of the decoded samples is larger than 10 counts (on a scale of 8031 counts) AND

2. The peak signal or noise level is smaller than the offset count.

Because the observed offset is masked in the presence of large signal amplitude, detection of offset requires that the encoder input be zero. (idle channel)

3.4.6 Real Time Bit Display

By setting the DISPLAY SELECT switch to BIT DSPL, the measurement section four 7-segment digits display the 8 bit binary value characterizing each sample in the selected channel. The sign bit, B1 corresponds to the leftmost bottom segment; the least significant bit, B8, corresponds to the rightmost bottom segment. Because the states are displayed in real time, the relative brightness of each segment represents a good approximation of the ratio of ones to zeros states over

time for each bit. As a consequency, a brightly lit segment indicates that the corresponding bit is in state one much more often than in state zero. The opposite is true for a dimly lit segment.

The examination of the binary code associated with each byte in the selected channel provides several useful indications:

1. when monitoring a VF signal, the examination of the real time bit display can reveal whether a bit is stuck (i.e. always at state one or state zero) and thus indicate a probable encoder malfunction.)
2. when monitoring a channel dedicated to data transmisssion, the state of the least significant bit (B8) indicates whether the channel is carrying traffic (B8 state one/lit) or is idle. In addition, several specific test or operational codes can readily be identified as a result of their repetition over a relatively long time.

3.5 OPERATING INFORMATION

This section aims at providing application related information which should facilitate the use of the model 320A+ for its intended purposes.

This section covers:

- Preparation for operation
- Monitoring mode
- Half channel transmission testing

3.5.1 Preparation for operation

The power switch is coupled with the volume control potentiometer 25 in figure 3.1. It may be either a pull-on/push-off switch or a rotary switch, depending on the version ordered. In the last case, power is turned on by twisting the volume control knob clockwise away from the minimum volume setting.

Upon power-up a microcontroller executes a comprehensive self-check procedure to ensure accuracy of the PCM event counting capability.

If the self test reveals no irregularity, the display flashes '8888' at a rate of once per second, indicating its readiness to start normal operation.

If a problem is discovered during the self test a specific diagnostic message is displayed and further event counting will not take place.

When the display flashes '8888', the operator must simultaneously press both momentary switches placed below the display (37 and 38 in Fig. 3.1) to clear all counters and initialize the slippage detector. Once cleared all counters are ready to accept event counts. During the execution of the self-test routine, the framing acquisition is disabled in both PCM diagnostic sections.

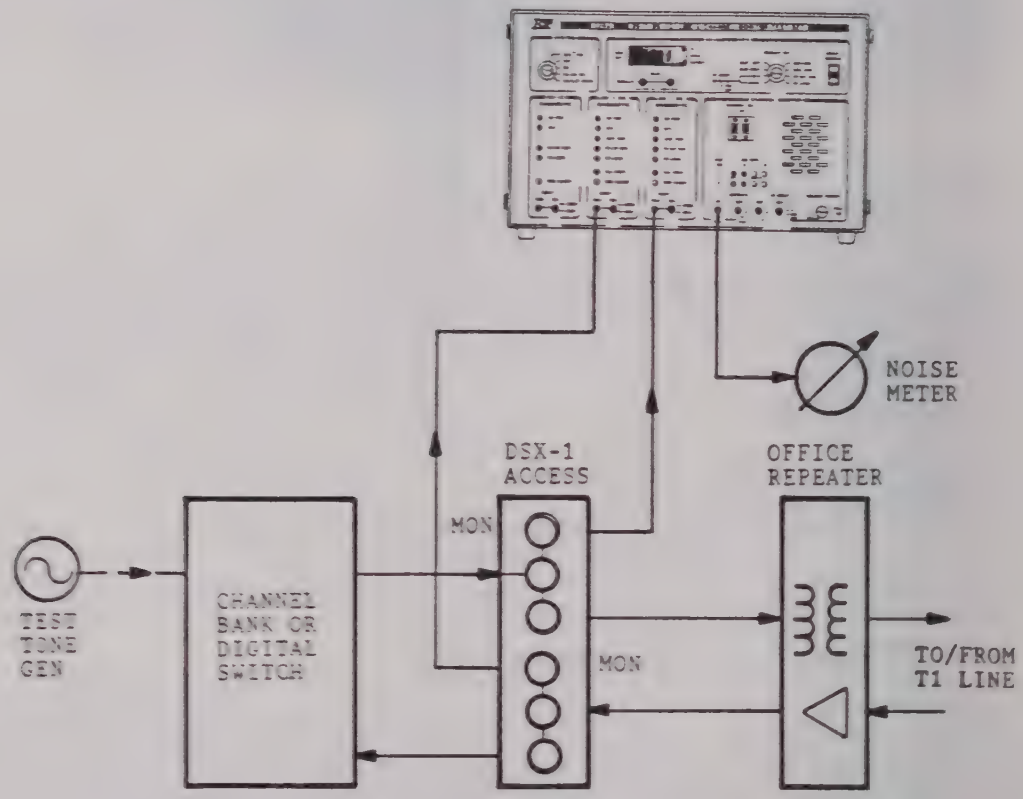

Fig. 3.5 PCM Monitoring Mode Set-Up

In the event of failure, as identified by the display of a diagnostic message, it is recommended to turn the power off and to restore it a moment later. This can sometimes clear a spurious problem.

3.5.2 Monitoring Mode

Figure 3.5 shows the basic DS1 monitoring configuration. In this mode either one or two PCM lines are monitored simultaneously; they may be for example the XMT and RCV pairs associated with a channel bank or they may be unrelated. When two lines are monitored simultaneously, this configuration allows for the observation of frame slippage as described in section 3.4.2. The frame slippage display provides the following information:

- determination of loop timing option selection in a channel bank while the bank is in service.
- evaluation of clock rate difference between two unrelated bit streams.
- determination of phase locking accuracy of the PCM signal clock transmitted through a higher level multiplexer.
- determination of a large amount of timing jitter in the transmission system.

Whether monitoring one or two lines, the 320A+ provides for half-channel transmission testing as described in the following sections.

3.5.3 Half-channel VF Transmission Testing

When the 320A+ is used along with a tone generator and a level/noise measuring set, both the transmit and the receive half-channel VF performance of D-type channel banks can be evaluated.

General test set-ups and procedures are provided for evaluating the transmit and receive half-channel parameters as follows:

Parameter	Chart No.
Gain	3-A
Gain Linearity	3-B
Frequency Response	3-C
Cross Talk (*)	3-D
Idle Noise (*)	3-E

* Transmit half-channel only.

Figure 3.6 shows the configuration to use for evaluating the VF transmit half-channel parameters; Figure 3.7 shows the corresponding configuration for the receive half-channel.

Notes:

1. When the noise/level meter is connected to the 320A+ VF output jack, it must present a 600 ohm nominal impedance to ensure level accuracy.

2. Proper allowance in the measurements must be made for the channel bank RCV level point as it may be different from 0dB.

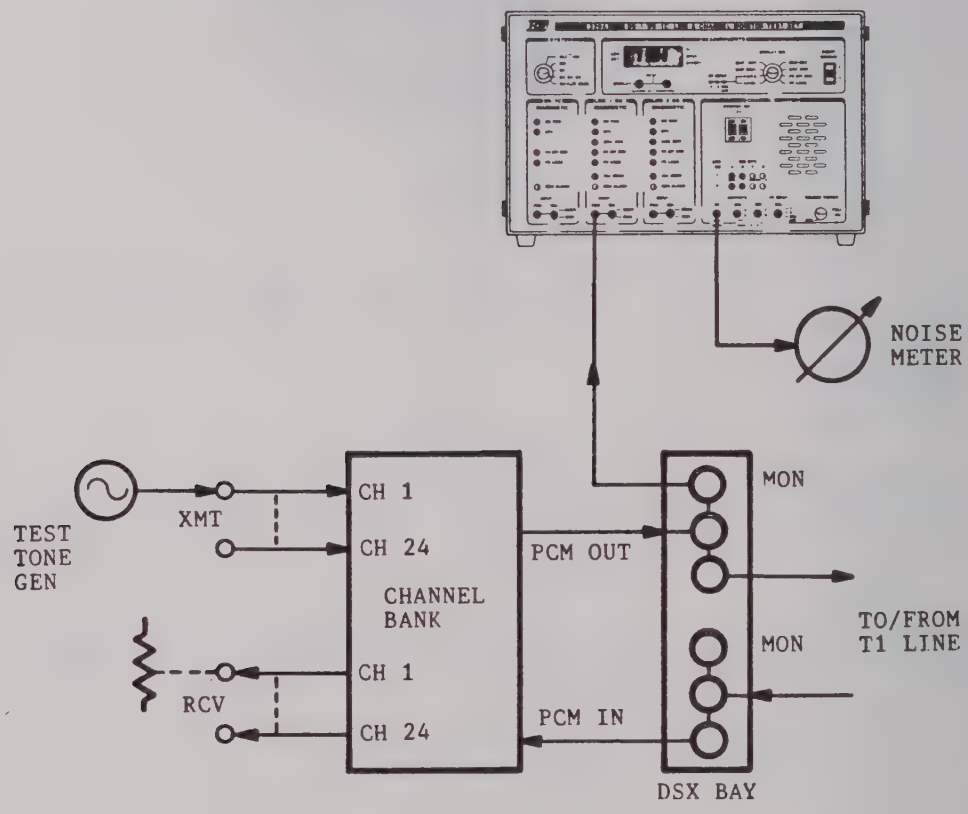

Figure 3.6 VF Transmit Half-channel Set-Up

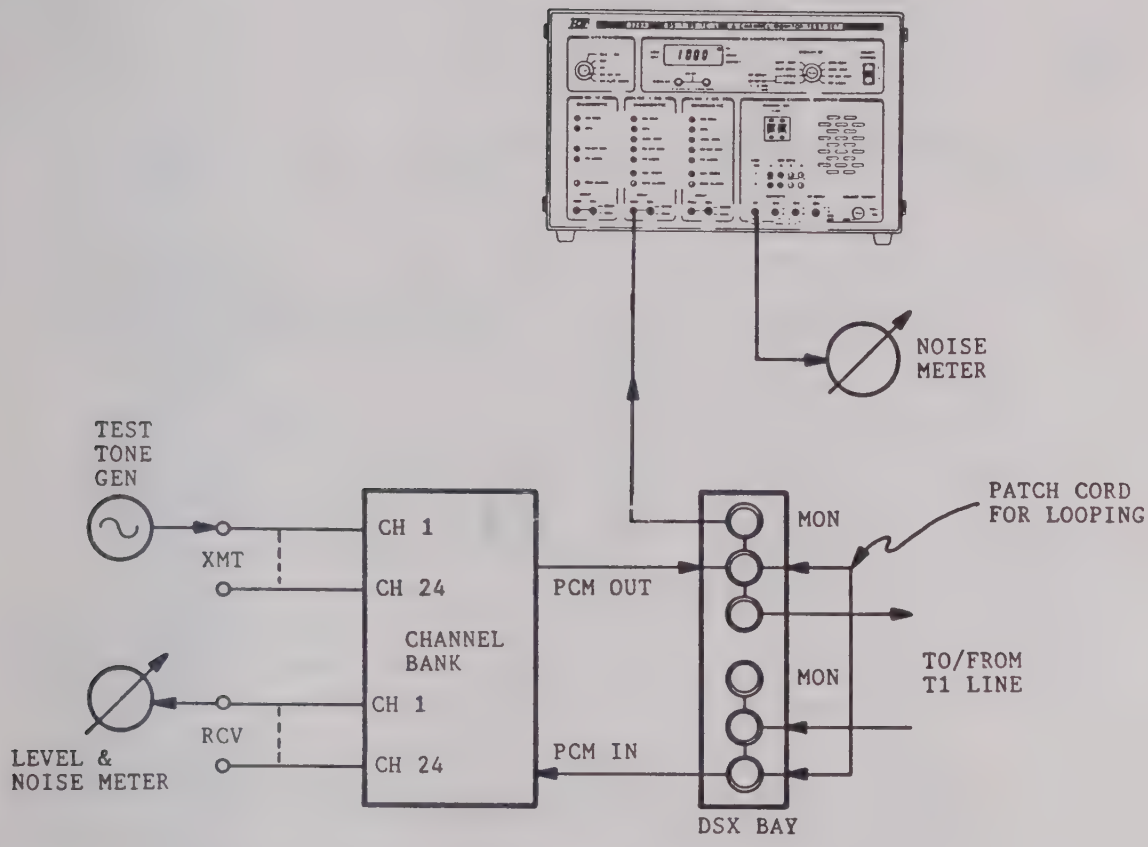

Figure 3.7 VF Receive Half-channel Set-Up

Chart 3-A

Gain Measurements

Step	Procedure
1	Set the tone generator controls as follows: - OUTPUT impedance to match channel input impedance - Frequency : 1010Hz +/- 5Hz - Level : 0.0dBm
2	Set the level and noise meter controls as follows: - Input impedance to match the channel unit output impedance - Level measurement
3	Set the 320A+ controls as follows: - System selection to match the type of D-bank - Channel selection to correspond to the channel number under test - Level measurement
4	Obtain the transmit gain by direct reading of the level in dB on the 320A+. (The channel unit receive port should be properly terminated).
5	Obtain the receive gain by subtracting the level in dB read on the 320A+ and on the level meter connected to the channel unit receive port.

Chart 3-B

Gain Linearity Measurements

Step	Procedure
1	Set the tone generator controls as follows: - Output impedance to match channel unit input impedance. - Frequency : 1010Hz +/- 5Hz - Level : 0.0 dBm
2	Set the level and noise meter as follows: - Output impedance to match the channel unit output impedance - Level measurement

Step	Procedure
3	Set the 320A+ controls as follows: - System selection to match the type of D-bank - Channel selection to correspond to the channel number under test - Level measurement
4	Obtain the transmit gain by direct reading of the level in dB on the 320A+ (the channel unit receive port should be properly terminated).
5	Obtain the receive gain by subtracting the level in dB read on the 320A+ and on the level meter connected to the channel unit receive port.
6	Repeat steps 4 and 5 after setting the tone generator level to other values in the range of +3 to -55 dBm0. (note that the channel bank encoder upper-level amplitude limit is +3.17dBm0.
7.	The gain linearity error is obtained by taking the difference between the tone generator level and the readings on the 320A+ and the level meter respectively.

Chart 3-C

Frequency Response Measurements

Step	Procedure
1	Set the tone generator controls as follows: - output impedance to match channel unit input impedance - frequency : 1010 Hz +/- 5Hz - level : 0.0dBm
2	Set the level and noise meter controls as follows: - input impedance to match the channel unit output impedance - level measurement
3	Set the 320A+ controls as follows: - System selection to match the type of D-bank - Channel selection to correspond to the channel number under test - Level measurement

4	Obtain the transmit gain by direct reading of the level in dB on the 320A+. (The channel unit receive port should be properly terminated).
5	Obtain the receive gain by subtracting the level in dB read on the 320A+ from the reading on the level meter connected to the channel unit receive port.
6	Set the tone generator frequency to other settings in the range of 200 to 4,000 Hz.
7	Repeat steps 4 and 5. The frequency response is obtained as the difference in dB between the reference level and the reading on the 320A+ and the level meter, respectively, for each selected frequency.

Chart 3-D

Crosstalk Measurements

Step	Procedure
1	Set the tone generator controls as follows: - output impedance to match channel unit input impedance. - frequency : 1010Hz +/- 5Hz - level : 0.0dBm
2	Set the level and noise meter controls as follows: - output impedance to match the channel unit output impedance when connected to the channel unit receive port or 600 ohm when connected to the 320A+ VF output jack - 'C' message noise weighting
3	Terminate the test channel transmit input port and the adjacent channel receive port with matching impedance.
4	Set the 320A+ controls as follows: - System selection to match the type of D-bank - Channel selection to correspond to the channel number under test
5	Obtain the transmit half-channel crosstalk by direct reading of the noise level on the noise meter connected to the 320A+ VF output jack.

Chart 3-E

Idle Half-Channel Noise Measurements

Step	Procedure
1	Terminate the input and output ports of the channel under test.
2	Set the 320A+ controls as follows: - System selection to match the type of D-bank - Channel selection to correspond to the channel number under test
3	Set the noise meter controls as follows: - Input impedance to 600 ohms - 'C' message noise weighting - connect the noise level meter input to the 320A+ VF output jack
4	Obtain the transmit idle noise by direct reading in dB on the noise meter.

Note: Since the 320A+ decoder idle noise is 13dBrnCo maximum, its contribution to this measurement can generally be ignored.

3.5.4 Half-channel Signaling Testing

When the 320A+ is complemented with a pair of signaling test sets both the transmit and the receive half-channel signaling performance of D-type channel banks can be evaluated.

General test set-ups and procedures are provided to evaluate the transmit and receive half-channel signaling as follows:

Type	Chart No.	Fig. No.
In-band signaling	3-F	3.8
E&M signaling	3-G	3.9

Chart 3-F

In-Band Signaling Measurements

Step	Procedure
1	Set the signaling test set send controls to deliver the desired tone level and frequency combination to the channel unit under test.
2	Set the signaling test set receiver controls to match the type of signaling corresponding to the sender selection.
3	Set the 320A+ controls as follows: - System selection to match the type of D-bank - Channel selection to correspond to the channel number
4	Verify signaling integrity by comparing the signaling delivered by the sender with the signaling obtained by each receiver.

Chart 3-G

E&M Signaling Measurements

Step	Procedure
1	Set the E&M signaling test set send controls todeliver the desired signaling state/number combination to the channel unit under test.
2	Set the signaling test set receiver controls as required to properly receive the sender selection.
3	Set the 320A+ controls as follows: - system selection to match the type of D-bank - channel selection to correspond to the channel number
4	Verify signaling integrity by comparing the signaling delivered by the sender with the signaling obtained by each receiver.

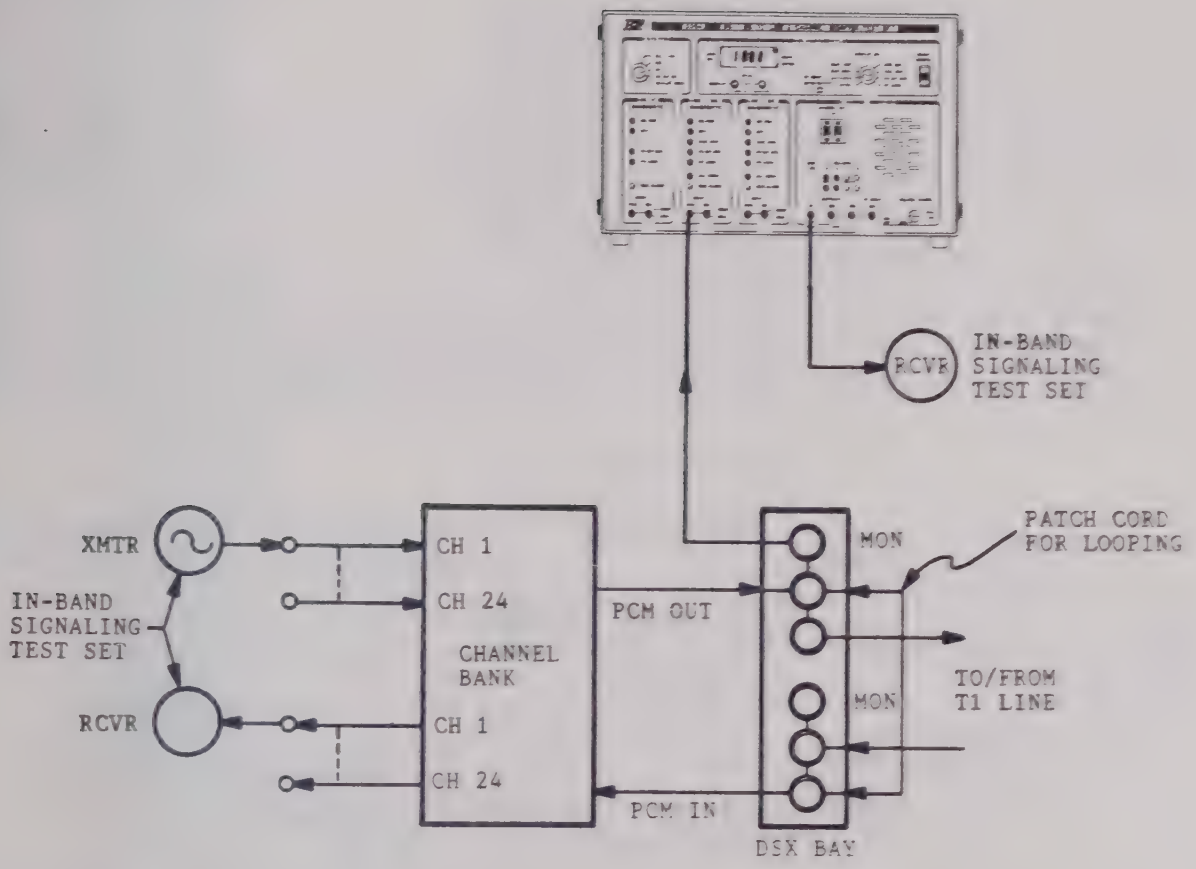

Figure 3.8 XMT/RCV Half-channel Test Set-up
for In-Band Signaling

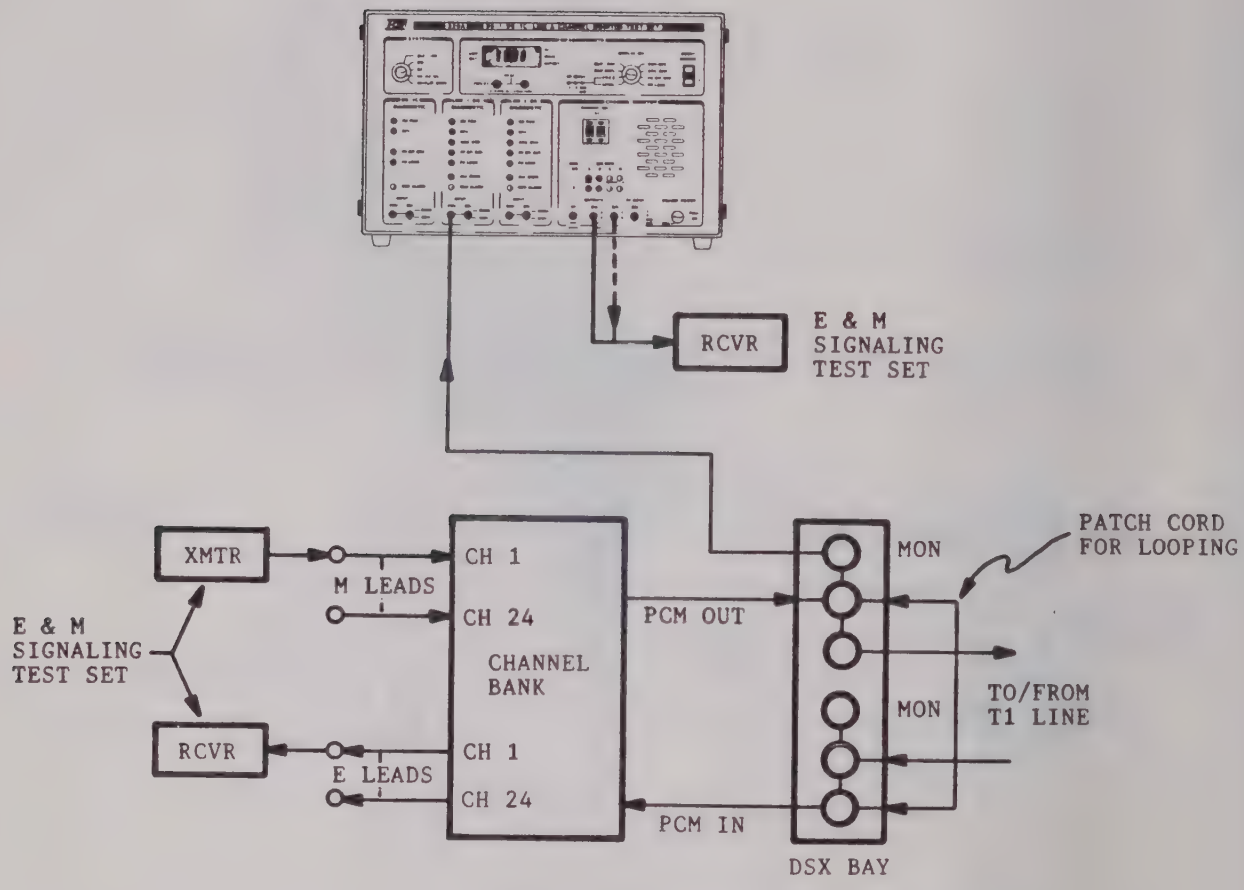

Figure 3.9 XMT/RCV Half-channel Test Set-up
for E&M Signaling

3.6 SELF-TESTING

As indicated in section 3.5.1, the 320A+ self-testing routine is executed automatically at power-up. This capability ensures that the event counting function, the display and the microcontroller operate properly.

A limited amount of additional testing can be performed by the user without requiring any additional equipment. This should be carried out prior to using the instrument, or when measurement difficulties are encountered. The procedure suggested below is not comprehensive; if a full performance check is required refer to section 6.

3.6.1 Testing Procedure

Initial Set-up

- Connect the 320A+ to the AC power line.
- Make sure no cords are plugged into any input-output jack.
- Set the system selection to 'D3/D4/D5'.
- Set the channel selection to '01'.
- Set the VF input selection to 'DIG mW'.
- Set the display selection to 'SLIP CNT'.
- Pull the volume control knob outward to power up.

Note the following conditions:

- DS1C diagnostic section:
  NO PCM and FR LOSS LED's lit.
- Line 1 and Line 2 diagnostic section:
  NO PCM and FR LOSS LED's lit.
- Display flashing '8888'.
- VF INPUT DIG mW LED lit.
- 1000 Hz pure tone is heard when volume control knob is set away from the fully counterclockwise position.
- All other LED's are off.

Reset the microcontroller by simultaneously depressing the two momentary switches located below the display.

Verify that all event counters are cleared:

- the display must read 0 when selecting COUNT SOURCE C and displaying SLIP CNT, BPV, ERR-SEC, FR BIT ERR and FR LOSS-SEC.
- the display must read 0 when selecting COUNT SOURCE 1 or 2, and displaying SLIP CNT, BPV, ERR-SEC, FR BIT ERR and FR LOSS-SEC for COUNT SOURCE 1 abd 2. [If the

system selection is not D5-ESF, the display should be '-00-' when selecting CRC ERR; if the instrument is not equipped for ESF operation (option 01), the display reads 'OP 1']

Verify that the display is blank when selecting SLIP DSPL.

Set the display selection to FREQ and observe the display to read 1000 +/- 1 Hz

Set the display selection to LEVEL and observe that the display reads 0.0 dBm0.

Set the volume control to the minimum.

Set the display selection to BIT DSPL and note that
- B2 and B3 are turned-off
- all other bits are neither fully on or fully off.

3.6.2 Self-Diagnostic/Display Messages

To help identify the location of the failure uncovered by the microcontroller self testing routine several messages can be displayed. Table 3.1 below identifies these messages along with their meanings.

Table 3.1 Self-Diagnostic Display Messages

Message	Corresponding Failure
E1 0	Line 1 BPV counter
E1 1	Line 1 CRC latch
E1 2	Line 1 FR LOSS & PCM FAULT latches
E1 3	Line 2 BPV counter
E1 4	Line 2 CRC latch
E1 5	Line 2 FR LOSS & PCM FAULT latches
E1 6	Line C BPV counter
E1 7	Line C FR LOSS & PCM FAULT latches
E1 8	frame slip latch
E1 9	Line 1 FR BIT ERR counter
E1 -	Line 2 FR BIT ERR counter
E1 E	Line C FR BIT ERR counter
E1 P	microcontroller EPROM checksum
E2 1	TMS processor PROM checksum

4. TECHNICAL DESCRIPTION

4.1 INTRODUCTION

This section provides a general description of the model 320A+ architecture and operation at the block diagram level.

4.2 ARCHITECTURE

The 320A+ is partitioned into six major sections which are interconnected as shown in figure 4.1 (next page):

1. DS-1C PCM Diagnostic
2. LINE 1 PCM Diagnostic
3. LINE 2 PCM Diagnostic
4. CHANNEL MONITOR
5. MEASUREMENTS
6. DS0 Interface (option 03)

The DS-1C PCM Diagnostic section displays any fault condition detected in the PCM input bit stream and demultiplexes this bit stream into the two D-groups DG1 and DG2. The data associated with each D-group is sent to Line 1 and Line 2 diagnostic sections, respectively. The detected fault events are sent to the Measurement section for storage into individual counters.

Each DS1 PCM Diagnostic section displays any fault condition detected in the PCM input bit stream and delivers to the Channel Monitor a replica of the PCM input along with the corresponding clocking, framing, and channel number data. Each PCM Diagnostic section also sends to the Measurements section the PCM recovered clock as well as data corresponding to each detected fault event.

The Channel Monitor provides the digital to analog conversion for the selected channel and delivers the VF level to the VF output jack. In addition, this section decodes and displays the signaling states associated with the selected channel content for both lines. The signaling states associated with the decoded VF level are also provided on dedicated jacks.

The Measurements section gathers data from the other sections and controls the readout to display the measurements in response to the operator's selection.

The DS0 Interface, option 03, receives appropriate timing related information along with the PCM content of the selected channel. This module delivers the content of the selected channel as well as two clocks needed to properly interpret this data.

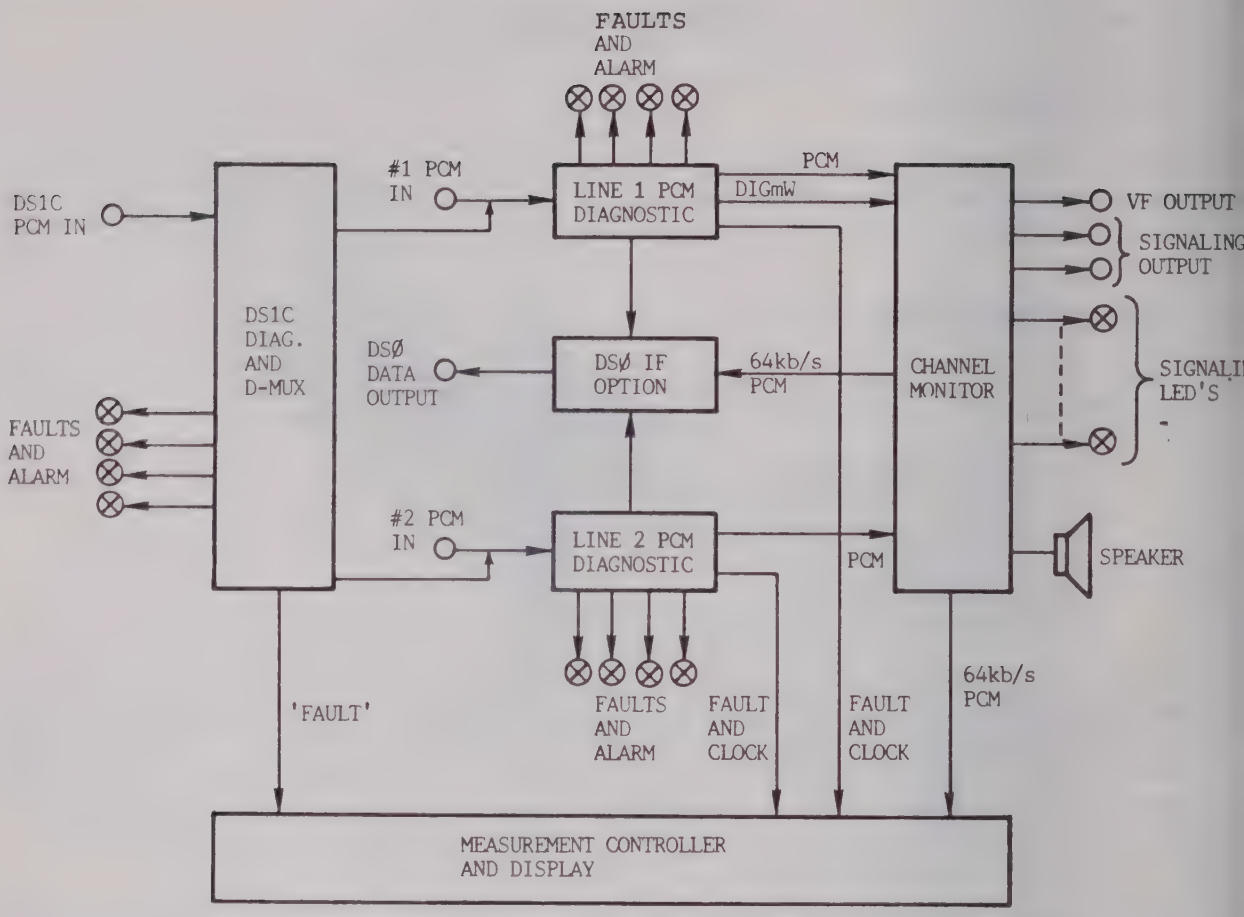

Figure 4.1 General Block Diagram

4.3 DS-1C DIAGNOSTIC SECTION BLOCK DIAGRAM

A simplified block diagram for the DS-1C PCM diagnostic section is shown in figure 4.2. The input PCM bit stream is terminated by the input conditioner according to the BRDG/MON selection. In turn, this circuit makes logic level decisions on the signal monitored and delivers a unipolar version of the signal to the clock recovery circuit, the NO PCM detector, the BPV detector, the framing processor and the de-stuffing and de-scrambling circuits.

The clock recovery circuit extracts the clocking information embedded in the input PCM bit stream. This clock signal is delivered to all circuits to ensure proper timing synchronization.

The fault detector detects and displays occurrences of bipolar violations (BPV's) and loss of carrier (NO PCM). Each occurrence of either event is captured by a latch under control of the measurement section.

The framing processor continually examines the incoming bit stream to capture and lock on the framing bit. Failure to acquire or to retain lock is displayed by the FR LOSS LED. Frame loss occurs when 2 out of 5 framing bits are in error. Except during frame loss, the framing processor displays individual frame bit errors. The framing processor provides for the synchronization of the remote alarm detector and the de-stuffing, de-scrambling circuits.

The remote alarm detector continually monitors the state of the 'X' bit. When this bit is '0', the REM ALARM LED is turned ON.

The de-stuffing and de-scrambling circuit provide the signal decoding required to restore the two originally encoded D-group bit rate and data content.

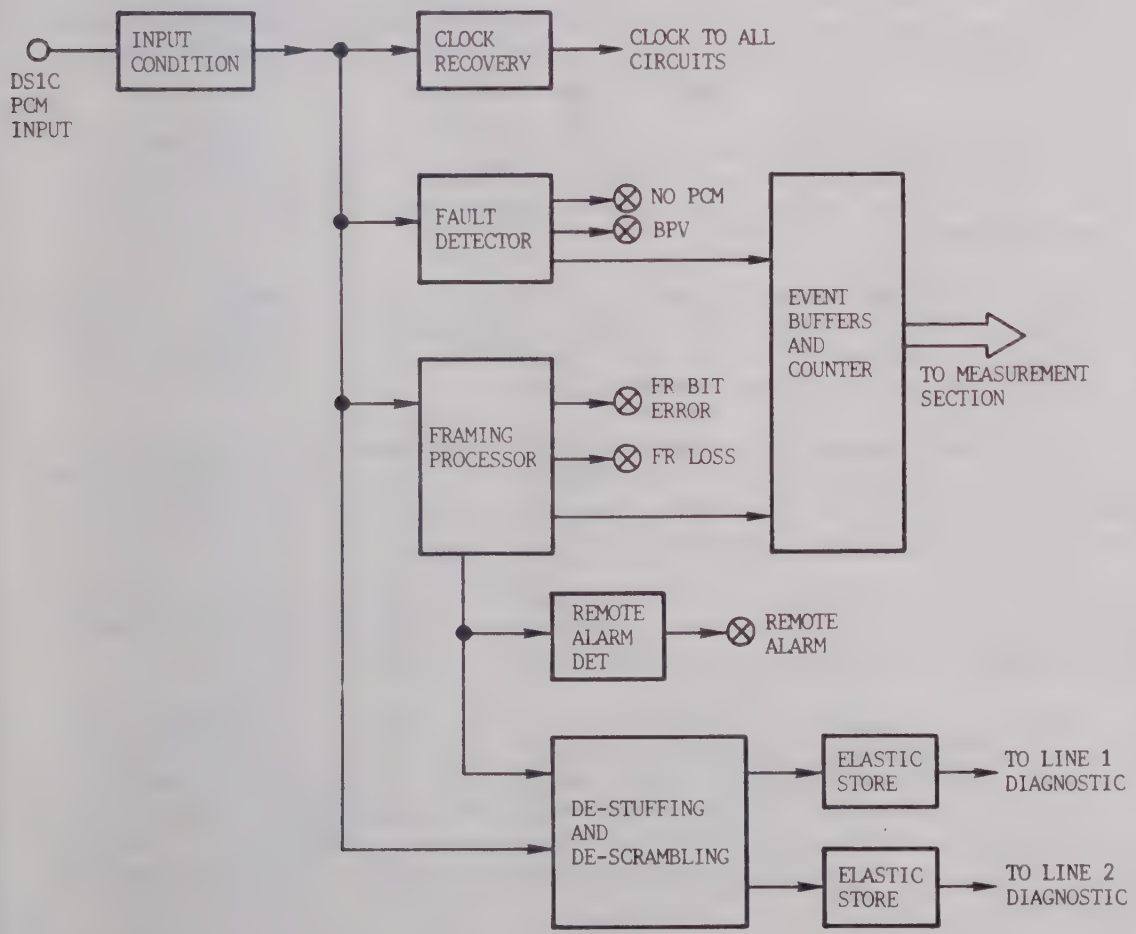

Figure 4.2 DS-1C Diagnostic/Demultiplex Section Block Diagram

The unipolar, de-stuffed data streams associated with D-group 1 and D-group 2 are processed by an individual elastic store to remove the bulk of the clock jitter resulting from the de-stuffing process. Removal of the jitter ensures accurate DS0 channel data recovery.

4.4 DS1 DIAGNOSTIC SECTION BLOCK DIAGRAM

A simplified block diagram for the two DS1 diagnostic sections is shown in Fig. 4.3. Although the two PCM diagnostic sections are identical, only the digital milliwatt generator associated with Line 1 is used.

The input PCM bit stream is properly terminated by the input conditioner. In turn, this circuit makes logic level decisions and delivers a replica of the received PCM to the clock recovery circuit, the fault detector circuit, the B8ZS code detector, the all-ones code detector, the framing processor and to the channel monitor section.

As its name indicates, the clock recovery circuit recovers the clock embedded in the input PCM bit stream. This clock signal is delivered in turn to most other circuits to ensure synchronization with the data.

The fault detector detects and displays occurrences of bipolar violations (BPV's) and loss of carrier (NO PCM). Each occurrence of either event is captured by a latch under control of the measurement section.

The B8ZS code detector detects the presence of the B8ZS code in the input PCM bit stream. When this code is detected, the corresponding LED is lit and BPV's associated with the code are neither displayed nor captured.

When the PCM input bit stream consists of an uninterrupted sequence of one bits for a minimum duration of 50ms, the all-ones detector causes the ALL ONES LED to light.

The framing processor circuit continually examines the incoming bit stream to capture and lock on the framing bit according to the system format selection. Failure to acquire or retain lock is displayed by the FR LOSS LED. Frame loss occurs when 2 out of 5 framing bits are in error. Except during frame loss, the framing processor calls for the display of individual frame bit errors.

When the ESF mode is selected, the CRC computer performs the polynomial division of the incoming PCM data and compares the remainder with the check bits sent by the PCM source. Failure

to match the remainder with the check bits results in flashing the CRC ERR LED and in alerting the framing processor.

Each occurrence of frame loss, CRC error and framing bit error is captured in a latch under control of the measurement section. When framing has been acquired, the framing processor synchronizes the digital milliwatt generator and the channel number sequence generator.

The digital milliwatt generator delivers a DS1 formatted bit stream containing the digital milliwatt code in each of the 24 channels. This bit stream is fed to the channel monitor section for self check purposes.

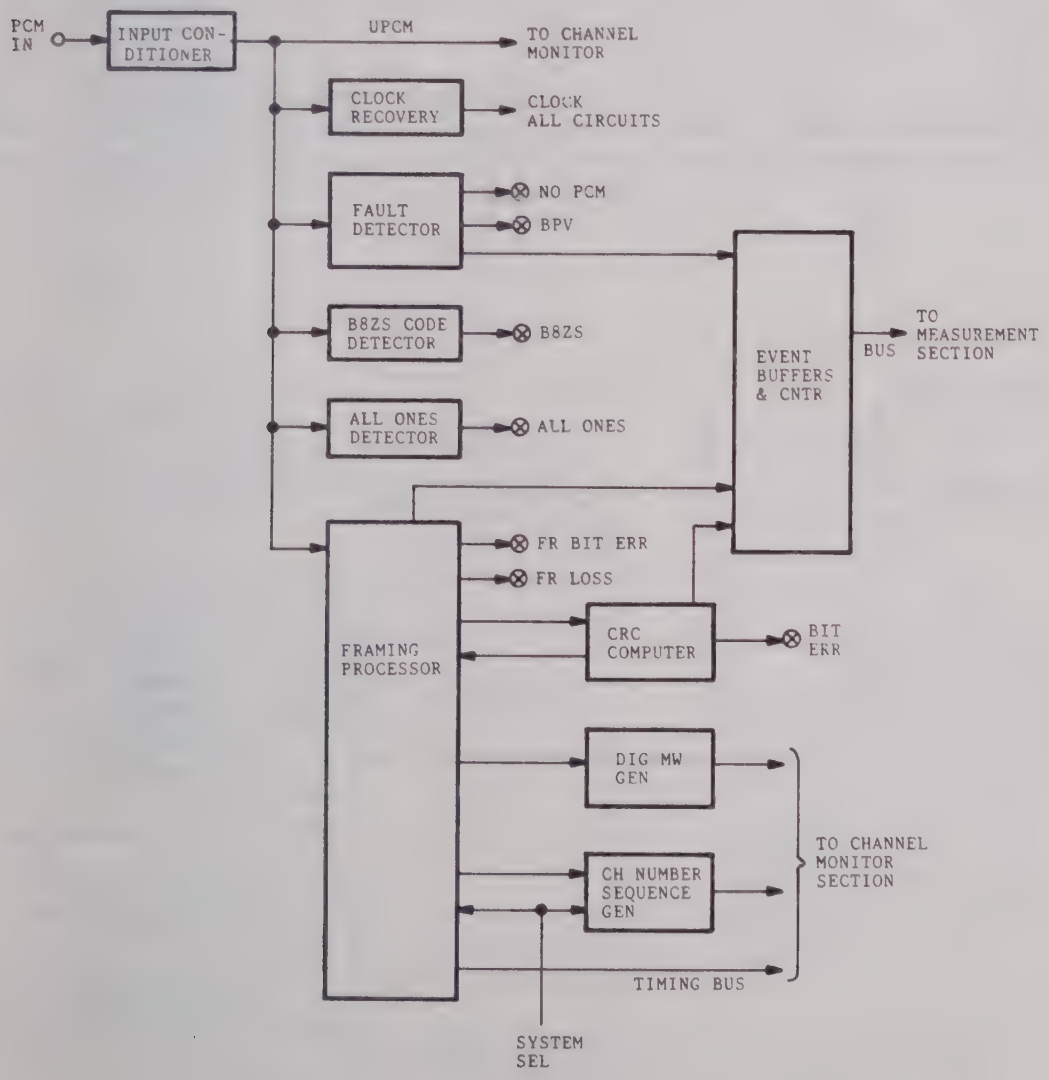

Figure 4.3 PCM Diagnostic Section Block Diagram

The channel number sequence generator, which is synchronized to the incoming bit stream, is fed serially to the channel monitor section to enable selection of individual channel contents. The numbering sequence is consistent with the system selection.

4.5 CHANNEL MONITOR SECTION BLOCK DIAGRAM

A simplified block diagram for the monitor section is shown in Figure 4.4.

The multiplexer (MUX) provides for the selection of the line to be monitored. The multiplexer output drives the magnitude comparator, the signaling state decoder-buffer, the D/A - VF decoder, and the measurement section.

The magnitude comparator compares the number encoded by the code switches with the instantaneous number obtained from the PCM diagnostic section channel numbering sequence

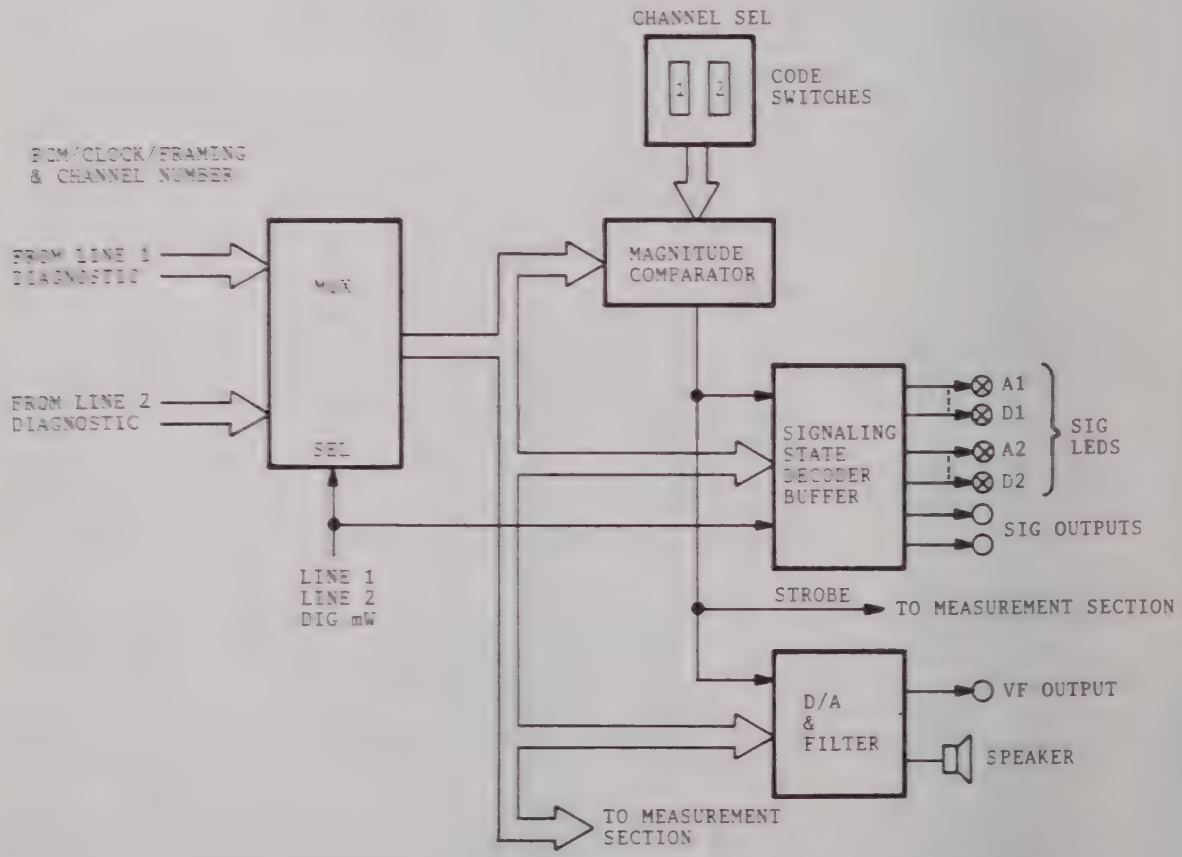

Figure 4.4 Channel Monitor Section Block Diagram

generator. When the two numbers are the same, the comparator delivers an enable signal to the signaling state decoder-buffer and to the D/A - VF decoder circuit.

The signaling state decoder-buffer provides for the decoding and display of the signaling states associated with the selected channel for each line monitored.

The D/A - VF decoder circuit provides the 600 ohm balanced VF output and feeds the speaker amplifier.

4.6 MEASUREMENT SECTION BLOCK DIAGRAM

A simplified block diagram for the measurement section is shown in Figure 4.5.

The microcontroller is at the heart of the measurement section. On a continuous basis, regardless of the display mode selection, it collects all the fault events associated with each PCM line monitored and the frame slippage detector and stores them into 15 individual counters.

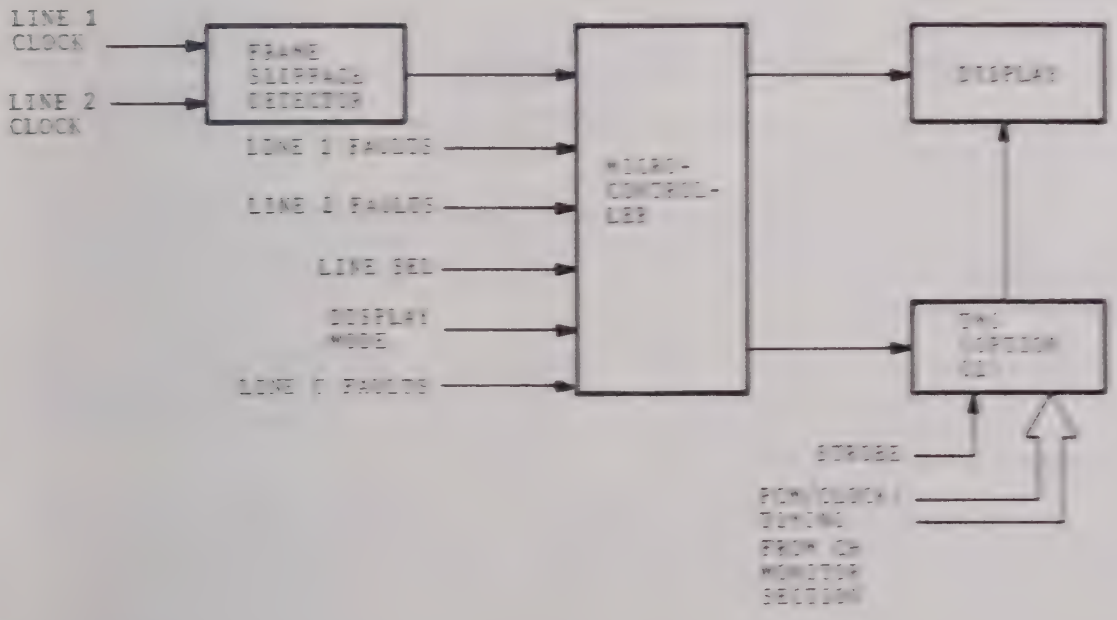

Figure 4.5 Measurement Section Block Diagram

In response to the display selection, the microcontroller controls access to the readout by the slippage detector and the TMS unit.

The frame slippage detector compares the frequency of the clock extracted respectively from Line 1 and Line 2 on an instantaneous basis. A series of thresholds corresponding to fractions of a full frame are compared with the detected slippage. As each threshold is reached a distinct LED segment is lit reflecting the instantaneous slippage.

When a full 125 microseconds of slippage has occurred, this condition is captured under the control of the microcontroller.

The display is driven from the microcontroller databus via a decoder and driver circuit.

The TMS capability operates under the control of the microcontroller. It consists of a distinct PC board assembly containing a special purpose digital processor circuit along with many peripheral devices. In response to the VF measurement selection, this circuit makes digital computations on the PCM samples corresponding to the monitored channel to determine either the level or the frequency of the signal and controls the readout to display the measurement in engineering units.

4.7 POWER SUPPLY SECTION BLOCK DIAGRAM

A simplified block diagram for the power supply section is shown in Figure 4.6.

The multiple voltages required by the instrument are provided by a DC/DC converter. This converter receives an unregulated DC voltage in the range of 11 - 18V and delivers four distinct regulated voltages.

If the input DC voltage falls below 11V, the converter is shut down and remains off until the DC voltage exceeds 15V. When in the off-state the converter presents a nearly infinite impedance to the DC source.

The unregulated DC voltage supplied to the DC/DC converter consists of either of two sources: the AC/DC converter or the battery supply (if option 04 is installed).

When AC is provided to the instrument the AC/DC converter provides the raw power to the battery charger to continuously float the battery.

If and when AC power is not provided, the battery charger allows the (charged) battery to provide the raw power to the DC/DC converter.

Low battery state of charge is detected by a low battery detector circuit. This circuit lights the low battery indicator when the battery charge is nearly depleted and to prevent deep discharge, it turns off the DC/DC converter when the battery's useful charge has been used up.

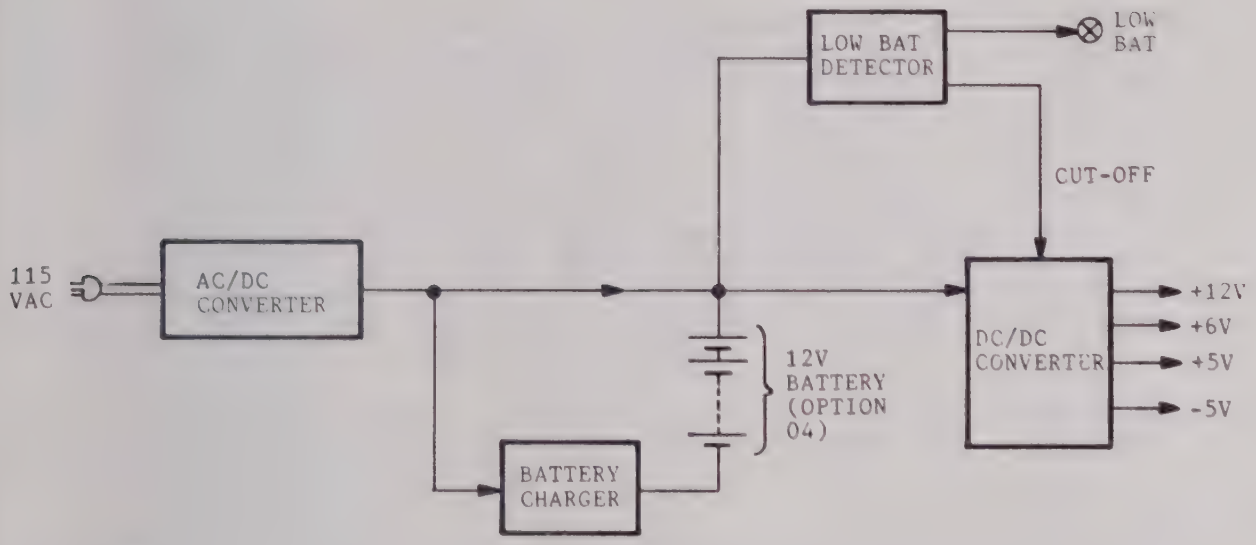

Figure 4.6 Power Supply Block Diagram

5. REAR PANEL ACCESS INTERFACE

5.1 INTRODUCTION

This section contains the information necessary for using the output interfaces provided on the 320A+ rear panel. This information includes a description of the electrical characteristics for each terminal.

5.2 ELECTRICAL INTERFACE DESCRIPTION

The electrical interface found on the rear panel consists of a 25-position female receptacle 'D-sub' connector and a 9-position female receptacle 'D-sub' connector. If the instrument is equipped with option 03, an additional bantam jack and a 5- position male connector are also provided.

The 25 position connector has two purposes: first it provides the means to access the messages contained in the data link associated with the SLC-96 and extended framing (ESF) transmissions; second, this connector provides all the signals required to slave the T-COM model 515A to the 320A+ when implementing the drop-and-insert mode.

The 9-position connector provides access to the signaling states associated with the monitored channel, simultaneously for both DS1 lines under test.

The bantam jack delivers the 64 kb/s data stream found in the selected channel in line 1 or line 2 as required for further processing by a data test set.

The five pin connector provides the timing signals required by the 64 kb/s data test set to properly decode the 64 kb/s data stream.

Detailed description for each of these connectors is found in tables 5.1 through 5.4 on the following pages.

TABLE 5.1
25 POSITION CONNECTOR PIN ASSIGNMENT

Pin No.	Identifier	Description
1	B8Z5*	Low state when B8Z5 code is detected
2	RPCM1	Recovered PCM from Line 1
3	GND	Ground
4	RCK1	Recovered clock from Line 1
5	D1D*	Low when D1D mode is selected

(TABLE 5.1 Continued)

6	1SYNCH*	System synchronization pulse consistent with Line 1 timing
7	-	Key
8	F_TTS1*	Pulse coincident with Ft on Line 1
9	SLC-96*	Low when SLC-96 mode is selected
10	RCK2	Recovered clock from Line 2
11	D5/ESF*	Low when D5-ESF mode is selected
12	RPCM2	Recovered PCM from Line 2
13	D3/D4/D5*	Low when D3/D4/D5 mode is selected
14	GND	Ground
15	-	No connection
16	-	No connection
17	-	No connection
18	D2*	Low when D2 mode is selected
19	FsTS1*	Pulse coincident with Fs on Line 1
20	FAULT1*	Low when PCM or framing is lost on Line 1
21	FsTS2	Pulse coincident with Fs on Line 2
22	FAULT2*	Low when PCM or framing is lost on Line 2
23	F_TTS2*	Pulse coincident with Ft on Line 2
24	2SYNCH*	System synchronization pulse consistent with Line 2 timing
25	ID	+5V/27 ohms

TABLE 5.2
9-POSITION CONNECTOR PIN ASSIGNMENT

Pin	Description
1	SIG A line 1
2	SIG B line 1
3	SIG C line 1
4	SIG D line 1
5	ground
6	SIG A line 2
7	SIG B line 2
8	SIG C line 2
9	SIG D line 2

TABLE 5.3
BANTAM JACK TERMINAL ASSIGNMENT

Terminal	Identifier	Description
Tip	Data	64 kb/s data
Ring	Data	64 kb/s data
Sleeve	GND	Ground/Sig. return

TABLE 5.4
5-POSITION CONNECTOR PIN ASSIGNMENT

Pin	Identifier	Description
1	GND	Ground
2	8KCLK	8 kHz clock
3	8KCLK	8 kHz clock complement
4	64KCLK	64 kHz clock
5	64KCLK	64 kHz clock complement

5.3 APPLICATION INFORMATION

The signals supplied by the 320A+ on the rear panel connectors comply in level, rate and timing relationship with the specifications outlined in section 5.4.

To implement the DS1 drop-and-insert operating mode, the 320A+ must be interconnected to the T-COM 515A using the T-COM cable P/N 2700-014. When this cable is connected, access to the data link messages is not feasable.

Access to the data link messages requires the capture of the message bits from the corresponding PCM bit stream. This can most easily be accomplished by combining the appropriate gating pulses shown in fig. 5.1 and the clock associated with this PCM stream to clock the message bits into a register.

By providing access to the signaling states associated with both lines, the 9-position connector enables the user to perform two different types of analysis:

1. Comparative Timing Measurements
   This type of measurement typically requires the use of an oscilloscope. By simultaneously monitoring the signal associated with various states, it is possible to

determine timing compliance with requirements. For example, if the A or B signaling states associated with each transmission direction are compared, one can determine during a call initiation phase the delay introduced by the far end system in sending back a wink. In addition, the wink duration can also readily be determined.

2. Call Statistics
   By connecting a strip chart recorder and monitoring the desired signaling states, it is possible to determine the number of attempted calls and the number of calls completed, as well as the duration of each call during the period of observation. Depending upon the type of signaling method used, it may even be possible to identify each number called.

The DS0 data is delivered in the logic format only. A strapping option on the DS0 access interface assembly is available to select either the true or the complement states. Because the data test set model KS20908 made by WECO requires the complement state, units are shipped with the complement selection. To change this selection the jumper placed between U7 and U11 on the DS0 interface board must be pulled out and installed in the NI (non-inverted) position.

The data associated with the monitored 64 kb/s channel is set to 00000000 when any of the following conditions prevails:

- No PCM on the monitored line
- Loss of framing on the monitored line
- Illegal channel number selection
- Selection of the internal digital mW

If it is preferred to obtain the state 11111111 for the data when any of the above listed conditions prevails, the jumper labeled M1 on the DS0 access interface must be removed.

CAUTION

To protect the timing signal drivers in the 320A+ it is recommended to limit the current drain to 10 mA on every output at all times.

5.4 ELECTRICAL INTERFACE SPECIFICATIONS

a. 25-Position Connector
   All signals and status leads on this connector interface with high speed CMOS logic circuits. When the load is purely capacitive and does not exceed 50 pF, the output logic levels are as specified below:

State	Level (Volts)
1	+ 5.0 ± .2
0	0.0 ± .2

Timing relationships between signals available on this connector are shown in fig 5.1 In this figure the clock period is 648 ns nominal with a duty cycle of 50% ± 5%. All signals are delayed with respect to the corresponding clock rising edge by 20 ns nominal.

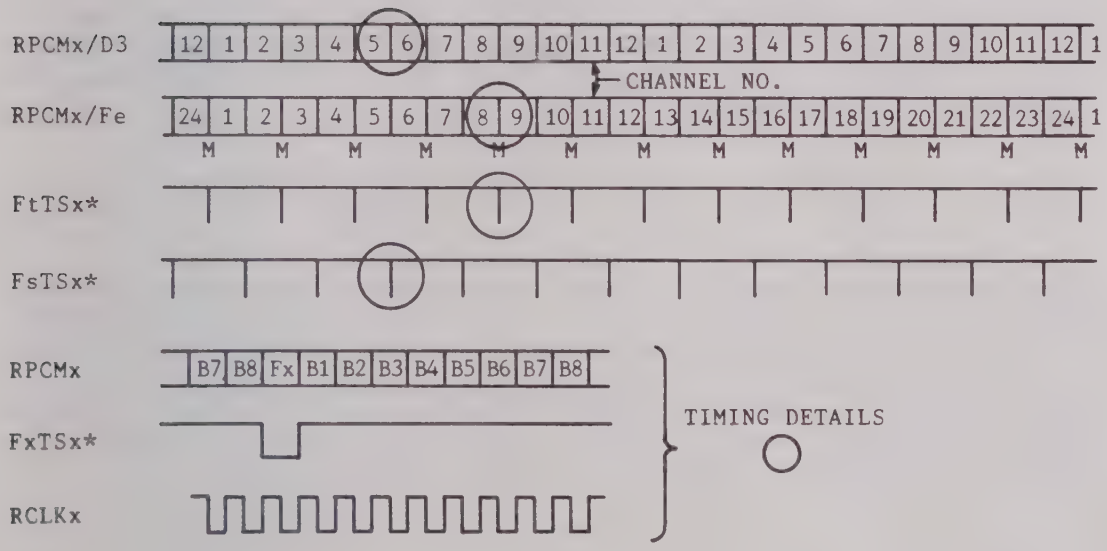

Fig. 5.1 Timing for 25 Position Connector

b. 9-Position Connector
With the exception of the ground terminal (5), all other terminals exhibit 3 states; these states are defined as follows in terms of the corresponding signaling state display LEDs:

State	LED Color	Nominal Level w/o Load
1	red	+ 1.6V
0	green	- 1.8V
no op	OFF	0.0V

The source impedance is 10,000 ohms for state 0 and 1; it is much larger than 10,000 ohms for no op.

The no op state occurs when any of the following conditions is obtained:
- framing is lost on the line associated with the signaling bit
- the channel number selected is illegal
- the state is not legitimate for the format selected (i.e., SIG C or D when the system selection is not D5-ESF)

c. Option 03 Connectors

The signals delivered by the 5 pin connector and the bantam jack are provided by a 74LS04 driver. The output logic levels listed below are applicable when the load does not exceed 10 TTLS devices.

State	Output Level (Volts)
1	2.4 min
0	0.5 max

Both phases of the 64 kHz and the 8 kHz clocks are provided. The duty cycle of the non-inverted 64 kHz clock is 5/8. The 8 kHz clock non-inverted phase has a duty cycle of 5/64. Fig. 5.2 shows the typical timing relationship existing between the clocks and the 64 kb/s data. The DSO data is normally delayed by approximately 20 ns with respect to the 64 kHz clock leading edge.

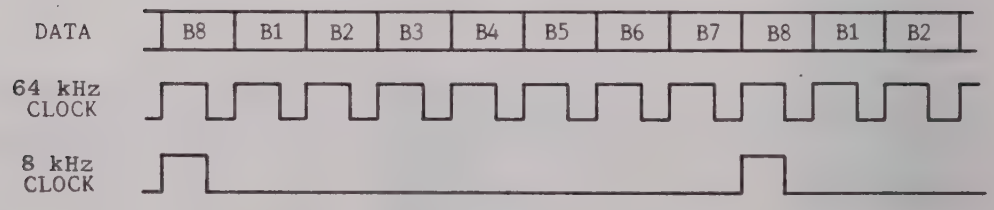

Fig. 5.2 Timing for DSO Connectors

5.5 ACCESSORY

The 9-position connector described in table 5.2 can mate with 9-pin D-subminiature connectors provided by several manufacturers. In particular, AMP Inc. supplies the following connector components:

AMP P/N	Description
745032-1	HDJ-20 receptacle housing
205311-9	HD-20 connector pin
207753-1	HDJ-20 plastic jacket
61831-1	strain relief
91234-1	insertion tool

T-COM can also supply a 4-foot, 9-conductor cable assembly. This cable (T-COM P/N 2700-021) is terminated at one end by the AMP connector above described and is left unterminated at the other end to suit the application.

6. ELECTRICAL PERFORMANCE CHECK

This section is in preparation. It will be included in the next issue of the manual, and will also be sent to those from whom T-COM has received the warranty card issued with this manual.

7. MAINTENANCE

This section is in preparation. It will be included in the next issue of the manual, and will also be sent to those from whom T-COM has received the warranty card issued with this manual.

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